MICROELECTRONICS EDUCATION: COMPARISON OF TWO DIFFERENT NMOS PROCESS

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ABSTRACT
This paper studies and compares two methodologies used for teaching undergraduate students about microelectronic. The evaluated methodologies are applied at University of São Paulo (USP) in Brazil and at Atelier Interuniversity of Micro and Nano Electronics (AIME) in France. Both methods provided an opportunity for students to participate of the fabrication and electrical characterization of silicon-gate nMOSFET technology. The USP/Brazil technology provides the possibility for the student to define the threshold voltage by ion implantation while in the AIME/France process no implantation step is used, resulting in a simpler process but limited.

Keywords
MOSFET technology, microelectronics education, transistor nMOS

1. INTRODUCTION
The MOS transistor (figure 1) is the most used semiconductor device for the fabrication of integrated circuits. However, a few universities offer to the students the opportunity to have contact with the CMOS fabrication process. This contact with the basic fabrication process steps as well as the devices electrical characteristics allows the students to have a wide vision about microelectronic field. It is important nowadays for the student to understand the relation between the electrical characteristics and the fabrication process steps. This work compares two approaches for teaching microelectronics fabrications, one done at University of Sao Paulo (USP/Brazil) and another at AIME/France.

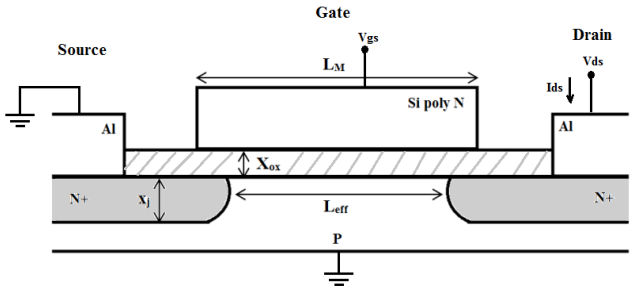


Figure 1 – Schematic cross section of nMOS Transistor

2. PROCESS DESCRIPTION
Both courses aimed to provide for students a general experience of the basic steps required in a MOS technology. The devices processed in course at AIME/France and the wafers have different NMOS circuits and devices such as diodes, capacitors, transistors and resistors, while the USP/Brazil process uses a chip test which contains resistors, diodes, capacitors and characterizations structures.

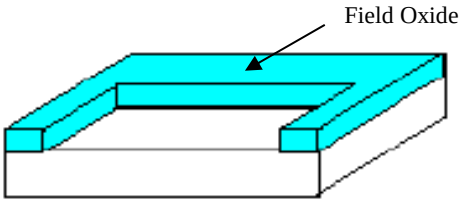
The AIME process is following detailed. More AIME/France process information can be found on reference [2]:

A) AIME/France: process steps
Wafer orientation (100) and $N_A = 9 \times 10^{15}$ cm^{-3}
1a. Field oxidation;
2a. 1st lithography: active area (figure 2-a);
3a. Gate oxidation;
4a. Poly-Si deposition by LPCVD;
5a. 2nd lithography: gate definition (figure 2-b);
6a. Source/drain and Poly-Si doping by diffusion;
7a. Deposition of SiO_2 by LPCVD;
8a. 3rd lithography: contact (figure 2-c);
9a. Deposition of aluminum by cathodic pulverization;
10a. 4th lithography: aluminum definition (figure 2-d);
11a. Sintering of aluminum.

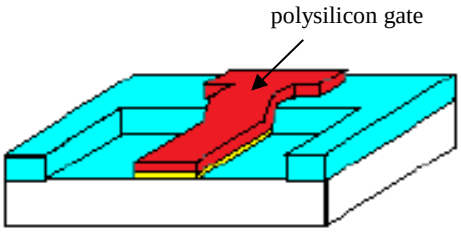
The second fabrication process presented was processed in course at Polytechnic School of USP/Brazil. The process steps are shown below:

B) USP/Brazil: process steps
Wafer orientation (100) and $N_A = 1 \times 10^{15}$ cm^{-3}
1b. Oxidation;
2b. Ion implantation of boron (V_{TH} adjust) designed by students;
3b. Deposition of SiO2 by PECVD technique (field oxide);
4b. 1st lithography: active area (figure 2-a);
5b. Gate oxidation;
6b. Poly-Si deposition by LPCVD and doping by diffusion;
7b. 2nd lithography: gate definition (figure 2-b);
8b. Ion implantation of phosphorus (source/drain);
9b. Deposition of SiO_2 by PECVD technique;
10b. 3rd lithography: Contact (figure 2-c);
11b. Deposition of aluminum by evaporation;
12b. 4th lithography: aluminum definition (figure 2-d);
13b. Sintering of aluminum.

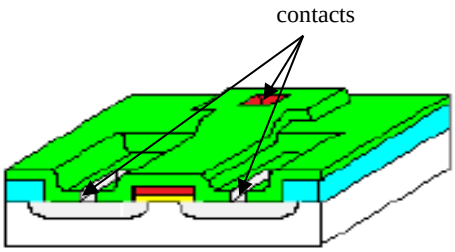
More USP/Brazil process information can be found on reference [3].
In both fabrication process are used the same 4 photo masks as can be seen in figures 2.
After each step of process fabrication, the students analyze the wafer in optical microscope to check the progress of process and operate characterization equipment's such as profilometer, elipsometer and four probe.
The final pictures of the chip fabricated using each microelectronic laboratory is shown in figure 3 (a and b).



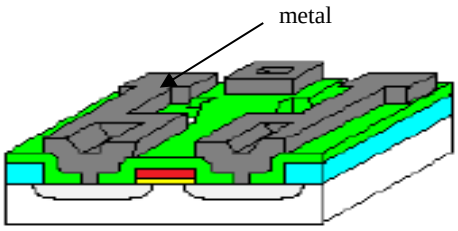
a) 1st lithography: Active area definition



b) 2nd lithography: Gate definition

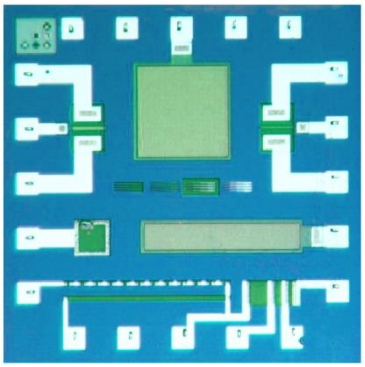


c) 3rd lithography: Contact definition

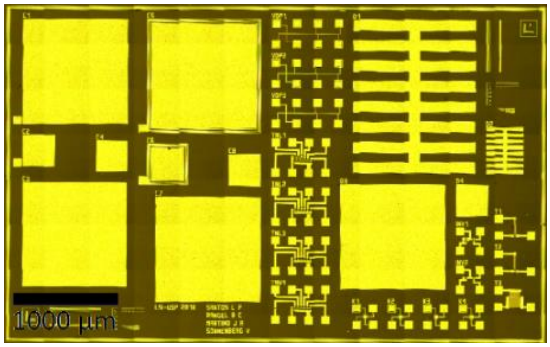


d) 4th lithography: Aluminum definition

Figure 2 – Litographys process steps



a) Chip fabricated by students (AIME/France)



b) Chip fabricated by students (USP/Brazil)

Figure 3 – Pictures of the chip fabricated by students

Table I resumes the main differences between both processes. USP/Brazil process uses the boron ion implantation (step 2b) in order to adjust the threshold voltage V_{TH} . Another important difference is the source/drain doping, which is performed at the AIME/France using diffusion step (step 6a), while USP/Brazil process uses ion implantation step (step 8b). The advantage and disadvantage of each fabrication process is discussed in Section 4.

Table I. Main differences of AIME and USP processes

nMOS – AIME/France	nMOS – USP/Brazil
-	Ion implantation of boron (V_{TH} adjust)
Source/drain diffusion	Ion implantation of phosphorus (source/drain)

3. ELETRICAL CHARACTERIZATION

The chip contains different characterization structures, such as Van der Pauw structures, Kelvin, diodes, capacitors, L-array and W-array transistors. In order to obtain better process fabrication, the main devices technologies characteristics were extracted using typical C-V and I-V curves. Figure 4 shows C-V curve of capacitor fabricated at USP/Brazil.

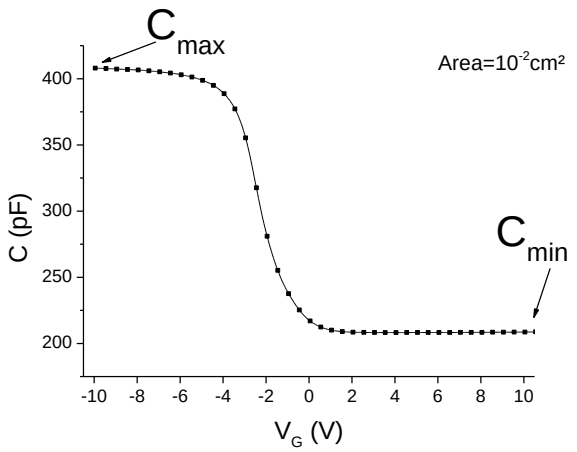


Figure 4 – Typical C-V curve of nMOS USP/Brazil

Extracting the maximum capacitance (C_{max}) from figure 4 it is possible to calculate the gate oxide thickness (X_{ox}) by equation 1 [4]:

$$X_{ox} = \frac{\varepsilon_{ox} * A}{C_{max}} \quad (1)$$

Where the $\boldsymbol{\varepsilon_{ox}}$ is the permittivity of SiO_2 and the **A** is the area. The effective impurity concentration (N_A) is calculated by equation 2 and the maximum silicon depletion width (d_{max}) can be obtained by equation 4 [4]:

$$N_A = \frac{4 * \varepsilon_{Si}}{q * d^2{}_{max}} * \varphi_F \quad (2)$$

$$\varphi_F = \frac{k * T}{q} * ln\frac{N_A}{n_i} \quad (3)$$

$$d_{max} = A * \varepsilon_{Si} * (\frac{C_{max} - C_{min}}{C_{max} * C_{min}}) \quad (4)$$

Where the $\boldsymbol{\varepsilon_{si}}$ is the permittivity of silicon, the $\boldsymbol{\varphi_F}$ is the Fermi level, the **k** is the Boltzmann constant, the **T** is the temperature in Kelvin, the **q** is the electron charge and $\mathbf{n_i}$ is the intrinsic carrier concentration in silicon at room temperature.

The typical drain current (I_{DS}) as a function of gate voltage (V_{GS}) curve is shown in figure 6. From these kind of curve it is possible to obtain some parameters like threshold voltage (V_{TH}), body factor constant (γ), carrier mobility (μ_0) and effective channel length (L_{eff}) [4].

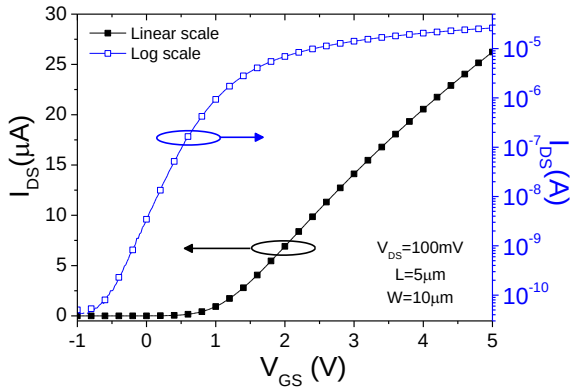


Figure 5 – I_{DS} x V_{GS} characteristic for nMOS fabricated at USP/Brazil

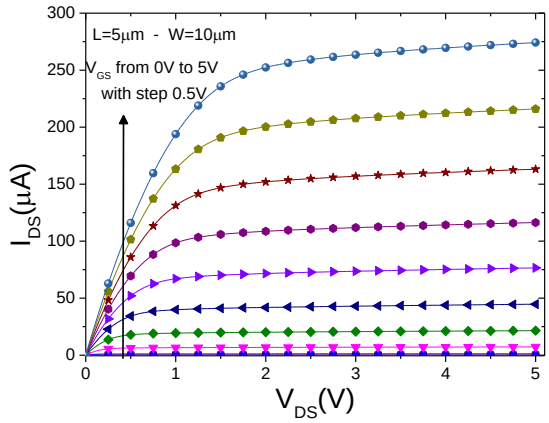


Figure 6 – I_{DS} x V_{GS} curve for nMOS fabricated at USP/Brazil

To obtain the threshold voltage (V_{TH}) we can use the linear extrapolation method [4], whereby a straight line is fitted to the linear drain current I_{DS} measured at low V_{DS} (typically 100 mV). The carrier mobility can be calculated from the maximum transconductance (gm_{max}) as shown in equation 5 [4]:

$$\mu_0 = \frac{L}{W * C_{ox} * V_{DS}} * g_{m_{max}} \quad (5)$$

The effective channel length consist the difference between the mask length and ΔL (equation 6), that occurs due to the lateral diffusion of dopants from source and drain into the channel, besides imperfections in lithography and corrosion steps.

$$L_{eff} = L_M - \Delta L \equiv \Delta L = L_M - L_{eff} \quad (6)$$

The body factor indicates the dependency between the threshold voltage and substrate polarization. The smaller the constant body effect, the smaller the variation of threshold voltage concerning the reverse substrate polarization will be. The smaller the constant body it is better and can be calculated by equation 7[4]:

$$\gamma = \frac{\sqrt{2 * q * \varepsilon_{si} * N_A}}{C_{ox}} \quad (7)$$

Table 2 shows the main extracted parameters for transistors fabricated at AIME/France and USP/Brazil.

Table 2 – Main experimental results of MOS

Parameters	AIME/France	USP/Brazil
X_{ox}	75,3 nm	80,8 nm
N_A	7,81 x 10^{15} cm^{-3}	1,54 x 10^{16} cm^{-3}
Q_{ss}/q	2,55 x 10^{10} cm^{-2}	4,43 x 10^{11} cm^{-2}
V_{TH}	0,78 V	1,25 V
γ	1,12 $V^{1/2}$	1,68 $V^{1/2}$
μ_0	686 $cm^2/V.s$	522 $cm^2/V.s$
ΔL	1,8 µm	1 µm
x_j	1,1 µm	0,8 µm

4. RESULTS AND DISCUSSION

From the experimental results showed in table 2 and the fabrication process steps presents on section 2 it is possible to see some differences that will be discussed in this section.

- Effective channel length ($L_{eff} = L_M - \Delta L$)

It is observed that the MOS AIME/France's ΔL is almost double to the USP/Brazil one. This occurs because the source/drain is gotten by diffusion. In the USP/Brazil process, the source/drain were obtained by ion implantation which makes it has a smaller junction P-N depth (xj), thereby obtaining a smaller ΔL, which is desirable. The disadvantage is to realize ion implantation it is necessary one more process, beyond to be a process that uses more sophisticated and expensive equipment, although the process used in the industry.

- Threshold voltage adjust (V_{TH})

In the USP/Brazil, threshold voltage can be defined by ion implantation of Boron step (step 2b) and in the AIME/France, V_{TH} depends only of the initial wafer doping. In the ion implantation process, it is possible to have a wide variation of this parameter with the same initial wafer. However this also results in a lower carrier mobility (μ_0) once that the doping concentration near the silicon/oxide interface becomes higher with degrades the μ_0.

- Effective oxide charge density (Q_{ss}/q)

The AIME/France presents an order of magnitude smaller than the USP/Brazil because at the USP laboratory, the cleanroom and the furnace is not dedicate exclusively for educational process.

- Carrier mobility (μ_0) and body factor (γ)

Since that the doping concentration (N_A) of the USP/Brazil process is higher, due to the ion implantation of Boron step, than AIME/France process, the body factor (γ) increase (equation 7) and the carrier mobility decreases as expected [4].

- Process Fabrication

The fabrication process used in AIME/France is simpler and cheaper because the ion implantation step is not used. However if the ion implantation equipment is available at the microelectronic laboratory, the USP/Brazil process is better because it permit the design on the V_{TH} of nMOS and higher effective channel length, which is used for more advanced technology.

5. CONCLUSIONS

In this paper, we analyzed the fabrication process and the main electrical characteristics of MOSFET devices obtained from two education microelectronics laboratories.

The conclusion is that both fabrication process are very useful for microelectronic education. The AIME/France is simpler and less expensive because the ion implantation equipment is not used. The source/drain in this case is defined by diffusion process .

The USP/Brazil process uses ion implantation, not only for designing the main transistor electrical characteristics which is V_{TH} but also for creating the source/drain regions, which is more compatible with the industry nowadays. If the ion implantation is available at the microelectronic laboratory, the USP/Brazil process is more indicated because it results in a updated device but if it is not, AIME/France process is the only way to fabricated microelectronics devices for education purposes.

The presented methods encourage the participation of the students in practice to verify what happens in theory. The practical training is needed for better absorption of knowledge and a brief visualization of industrial processes. Depending on the application, it is possible to present the practice formation of two ways, according to the procedures described in this paper. At the end of the course the students take home the chip designed and fabricate during the course.

6. ACKNOWLEDGMENTS

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7. REFERENCES

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