Behavior Investigation of trench-gate and vertical diffusion power MOSFET

F. O. Dainese[1], J. W. M. Santiago[1], M. Kawano[1,3], E. Pfeifer[1,2], D. A. Arrabaça[1], M. Rodrigues[1] and M. Galeti[1]

[1]Centro Universitário da FEI - São Bernardo do Campo, Brasil

[2]SMS / Legrand – Diadema, Brasil

[3]Universidade de São Paulo – São Paulo, Brasil

ABSTRACT

This work presents an analysis of the power MOSFET transistor made in two different topologies, vertical diffusion and trench gate. It was observed that trench gate MOSFET can achieve a reduced on-resistance and a larger gate capacitance. Additionally, an improved transconductance and a larger breakdown voltage were seen. Moreover, the impact of larger lifetime carriers on the breakdown voltage was also analyzed on these devices, indicating to be very sensitive and reduced with this parameter increase.

Keywords

Microelectronics, Power MOSFETs, vertical diffusion MOSFETs, trench gated MOSFETs.

1. INTRODUCTION

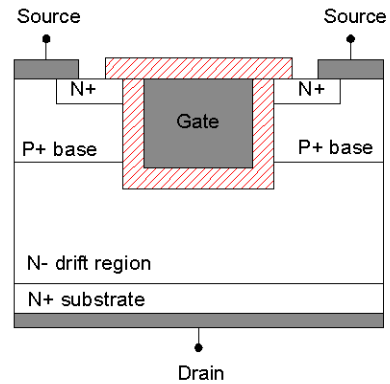
The power metal–oxide–semiconductor field effect transistors (MOSFETs) has been widely used in DC-AC converters and in power supplies thanks to their low conduction power loss, high input impedances and high switching speed capabilities. Among different power devices the vertical diffusion VD-MOSFET (the manufacturing process of the P wells are obtained by a diffusion process) that was developed in the mid-1970s, was introduced aiming to improve performance when compared with the well-known power bipolar transistors [1]. The vertical power MOSFETs were initially considered to be ideal power switches due to their high input impedance and switching speed. However, their power-handling capability was constrained by the internal resistance within the structure between the drain and source electrodes. The power dissipated due to the voltage drop in the internal resistance limited the current-handling capability of the power MOSFETs as well as the efficiency of the power circuits in which they were utilized. An alternate device structure known by trench-gate or U-MOSFET was also developed in the 1990s [2]. This structure enabled an increase in the operating frequency for power MOSFETs to the 1-MHz range [3].

The motivation for this work is to investigate the main differences between these two topologies: VD and power U-MOSFET. This analysis was conducted by numerical simulations, and parameters as on-resistance and breakdown voltage were investigated.

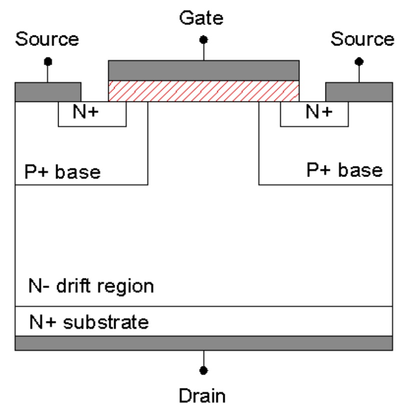
2. NUMERICAL SIMULATIONS

A cross-section of the basic cell structure for the vertical-diffused (VD) MOSFET and the trench-gate or U-MOSFET structure are illustrated in Fig. 1. As shown, U-MOSFET structure extends from the upper surface of the structure through the N+ source and P-base regions into the N-drift region. The gate electrode is placed within the trench after the formation of the gate oxide by thermal oxidation of the bottom and sidewalls.

Two-dimensional numerical simulations were performed using the Atlas (SILVACO) [4]. The power MOSFET transistors analyzed in this paper were simulated with the parameters presented on table I.



(a)



(b)

Figure 1 – Schematic cross-section of a (a) U-MOS and (b) VD-MOS power transistors.

Table 1 – Typical parameters for the VD and U-MOS structures used in the simulations.

Parameter	Value	Unit
N+ substrate thickness	10	µm
N- drift thickness	158	µm
P-base thickness	8	µm
N+ source regions thickness	1	µm
N+ substrate width	25	µm
N- drift width	25	µm
P-base width	8	µm
N+ source width	6	µm
N+ substrate doping	5E19	cm^{-3}
N- drift doping	2E15	cm^{-3}
P-base doping	5E16	cm^{-3}
N+ source regions doping	1E20	cm^{-3}
Trench width	13	µm
Trench thickness	10	µm
Gate oxide thickness	40	nm

3. SIMULATIONS RESULTS

3.1 Gate capacitance

Gate capacitance was simulated for both power MOSFETs, and as can be seen on Fig. 2 a larger capacitance is observed for the U-MOS structure. This is related with the larger gate area presented on this structure. Fig. 3 presents the schematic cross-section of U-MOS and VD-MOS power transistors indicating the channel length (L) position. As can be seen, the gate oxide is larger for U-MOS transistors.

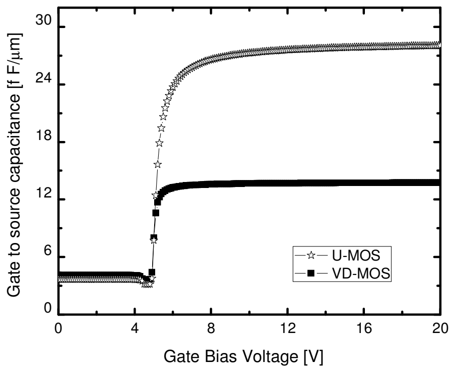


Figure 2 – Gate capacitance behavior for the different power MOS transistors.

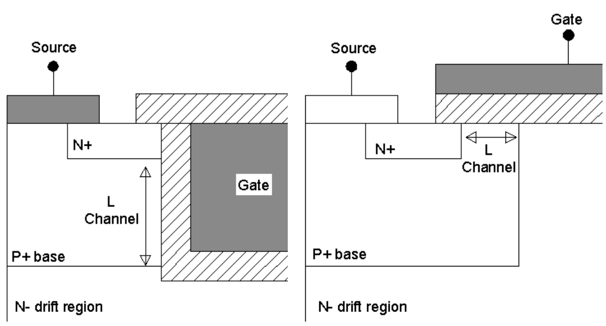


Figure 3 – Schematic cross-section of a (a) U-MOS and (b) VD-MOS power transistors indicating the channel length.

3.2 On-resistance

The on-resistance (RON) for a power MOSFET structure is defined as the total resistance to current flow between the drain and source electrodes when a gate bias is applied to turn on the device. Fig. 4 presents the on-resistance extracted from IDS x VDS curves for the different structures. U-MOS transistors can achieve a reduced on-resistance. In order to analyze this behavior, Fig. 5 presents the internal resistance components for the two structures. The same internal resistances found in the power VD-MOSFET structure are presented in the power U-MOSFET structure with the exception of the N region resistance under the gate (RJFET) [5]. This region is eliminated within the power U-MOSFET structure because the trench extends beyond the bottom of the P-base region to form a channel connecting the N+ source region with the N-drift region [6,7]. The elimination of this region allows a significant reduction of the overall specific on-resistance for the power U-MOSFET structure [8].

3.3 Transconductance

Fig. 6 presents the normalized transconductance by gate area extracted for the different MOS structures as a function of the temperature. U-MOS structures present a larger transconductance for all the temperature range analyzed. It is known that the transconductance is dependent of the gate oxide capacitance. As a result the larger transconductance for U-MOS structures is related with the larger gate oxide capacitance observed on these structures. Larger drain current was also observed on this structure.

3.4 Breakdown voltage

The breakdown voltage of a power semiconductor device is one of its most important characteristics. Together with its maximum current handling capability, this parameter determines the power rating of the device [9]. Basing on that the breakdown characteristics were simulated comparing the different MOSFET structures (Fig. 7).

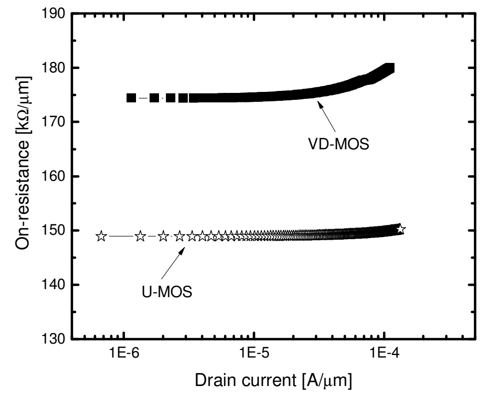
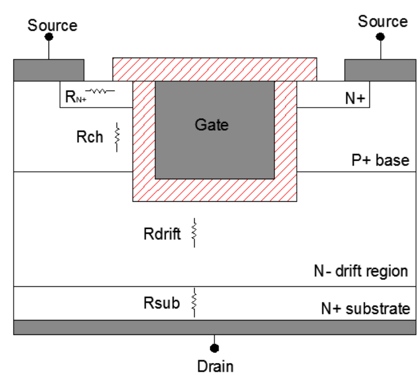
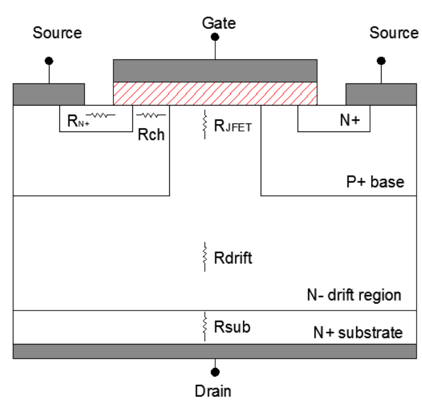


Figure 4 – On-resistance behavior for the different power MOS transistors.



(a)



(b)

Figure 5 – Schematic cross-section of a (a) U-MOS and (b) VD-MOS power transistors indicating all the resistance components.

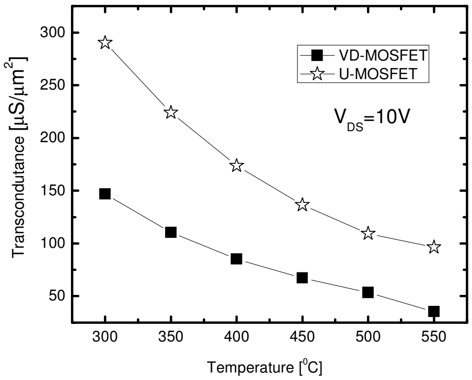


Figure 6 – Transconductance extracted for the different power MOSFET structures as a function o the temperature.

It is possible to observe that U-MOS structures can achieve a larger breakdown voltage (85V) than the VD-MOS (60V). It is known that the leakage current observed for VGS=0V is proportional with the junction area. As the U-MOS structure presents a reduced junction area thanks to the trench gate, a reduced drain current level can be observed in comparison with the VD-MOS structure. This larger drain current level leads to an increased impact ionization reducing the breakdown voltage for VD-MOS.

Fig. 8 presents the drain current as a function of the drain bias, for different MOS structures and lifetime carriers, during operation in the blocking mode (VGS=0 V). It is known that the leakage current observed for VGS=0V is proportional with the junction area. As the U-MOS structure presents a reduced junction area thanks to the trench gate, a reduced drain current level can be observed in comparison with the VD-MOS structure. This leakage current is inverse dependent to the lifetime carriers, as a result it is possible to observe that with the increase on the effective lifetime carriers (TAUN+TAUP/2) a reduction on the leakage current level for the same MOS structure. Another important point is related to the reduced breakdown voltage with the increased lifetime carriers. The power MOSFET structure contains a parasitic bipolar transistor formed between the N+ source region, the P-base and the N-drift region [10]. With the increase on the lifetime carriers, it is known that the current gain of the N-P-N bipolar transistor is enhanced. As a result, a reduction in the breakdown voltage is observed for larger lifetime carriers.

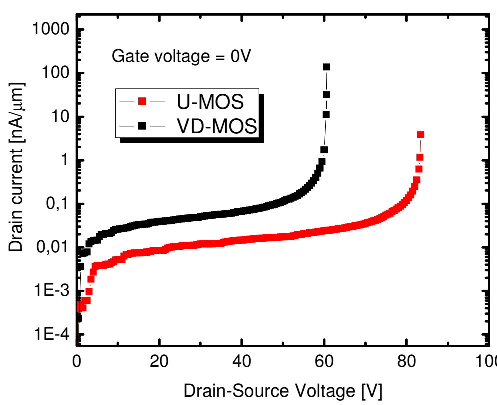


Figure 7 – Simulated breakdown characteristics.

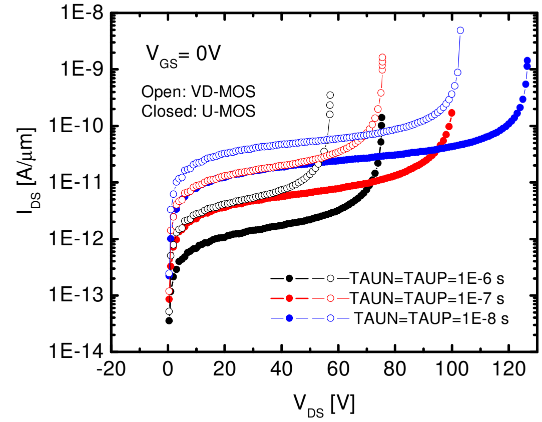


Figure 8 – Simulated breakdown characteristics for different lifetime.

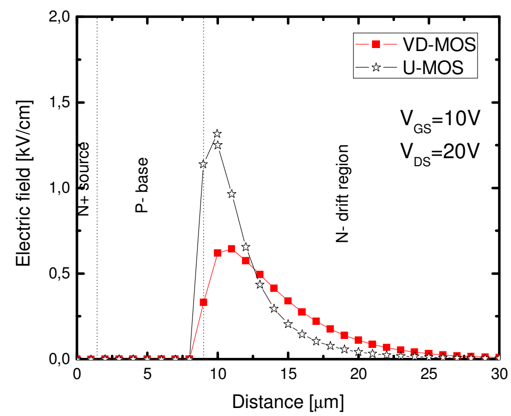


Figure 9 – Simulated electric field for the different MOS structures.

The electric field (Fig. 9) was also extracted in order to better understand the breakdown behavior, for both structures, a gate voltage of 10V and drain bias of 20V. The electric field was extracted on the vertical direction near the trench gate oxide. It is possible to observe a larger electric field for the U-MOS transistor near the gate oxide. This behavior is related with the reduced distance between the gate/drain electrode for these devices and knowing that the electric field is inversely proportional to this distance.

4. CONCLUSIONS

This paper compared different power MOSFET structures through numerical simulations. It was analyzed the Trench-gate (U-MOS) structure and the conventional VD-MOS. Initially it was observed a larger gate capacitance for U-MOS devices that are related with the larger gate area due to the trench-gate. This capacitance also impacts on the on-resistance where the trench-gate or U-MOSFET structure offered the opportunity to reduce the internal resistance of the power MOSFET. The breakdown voltage was also extracted during operation in the blocking mode for both structures and it was observed that U-MOS transistors can achieve a larger breakdown voltage. This phenomenon is related to the reduced junction area thanks to the trench gate. This leads to a reduced drain current level, and consequently larger impact ionization is seen, resulting in this increased breakdown voltage. Finally, the influence that the lifetime carriers cause on the breakdown voltage was also analyzed. It was observed that a reduced breakdown voltage can be achieved for larger lifetime carriers due to the enhanced current gain of the N-P-N transistors.

5. ACKNOWLEDGMENTS

Michele Rodrigues and Milene Galeti would like to thank to the Brazilian research-funding agency FAPESP for the support for developing this work.

6. REFERENCES

[1] D.A. Grant and J. Gowar, "Power MOSFETs: Theory and Applications", Wiley, New York, 1989.

[2] B.J. Baliga, "The Future of Power Semiconductor Technology", Proceedings of the IEEE, Vol. 89, pp. 822–832, 2001.

[3] B.J. Baliga, "Power Semiconductor Device Figure of Merit for High Frequency Applications", IEEE Electron Device Letters, Vol. EDL-10, pp. 455–457, 1989.

[4] Atlas. Users manual, Silvaco (2007

[5] C. Hu, M.-H. Chi, and V.M. Patel, "Optimum Design of Power MOSFETs",IEEE Transactions on Electron Devices, Vol. ED-31, pp. 1693–1700, 1984.

[6] S.C. Sun and J.D. Plummer, "Modeling of the On-Resistance of LDMOS,VDMOS, and VMOS Power Transistors", IEEE Transactions on Electron Devices, Vol. ED-27, pp. 356–367, 1980.

[7] T. Syau, P. Venkatraman, and B.J. Baliga, "Comparison of Ultra-Low Specific On-Resistance U-MOSFET Structures: The ACCUFET, EXTFET, INVFET, and Conventional U-MOSFETs", IEEE Transactions on Electron Devices, Vol. ED-41, pp. 800–808, 1994.

[8] D. Kinzer, D. Asselanis, and R. Carta, "Ultra-Low Rdson 12 V p-Channel Trench MOSFET", IEEE International Symposium on Power Semiconductor Devices andCs, pp. 303–306, 1999.

[9] B.J. Baliga, "Power Semiconductor Devices Having Improved High Frequency Switching and Breakdown Characteristics", U.S. Patent 5,998,833, December 7, 1999.

[10] J. Zeng et al., "An Ultra Dense Trench-Gated Power MOSFET Technology Using a Self-aligned Process", IEEE International Symposium on Power Semiconductor Devices and ICs, pp. 147–150, 2001.