Automatic Design of Fully Differential Amplifiers With Common-Mode Feedback

Arthur C. Oliveira
Federal University of Pampa
Computer Archtecture and Microelectronics Group
Alegrete-RS, Brazil
arthuroliveira@alunos.unipampa.edu.br

Lucas C. Severo
Federal University of Pampa
Computer Archtecture and Microelectronics Group
Alegrete-RS, Brazil
lucas.severo@unipampa.edu.br

Alessandro G. Girardi
Federal University of Pampa
Computer Archtecture and Microelectronics Group
Alegrete-RS, Brazil
alesandro.girardi@unipampa.edu.br

ABSTRACT

Fully Differential amplifiers play a critical role in systems which differential signaling is present. One drawback of designing this kind of circuit is the need of an extra circuit to keep it stable. This paper presents a methodology for automatic design of fully differential amplifiers with output balance considering both main-amplifier and common-mode feedback (CMFB) circuits. The methodology is divided in two parts: first, the main amplifier is designed using an ideal CMFB; then, based on the obtained results, the CMFB is designed separately. This strategy improves the convergency of the optimization algorithm since the design space is reduced. Simulation results show that the fully differential amplifier with a continuous CMFB circuit achieves a satisfactory solution, thus showing the suitability of the methodology for automatic design.

Categories and Subject Descriptors

B.7 [**INTEGRATED CIRCUITS**]: Design Aids—*automatic design, fully differential, common-mode feedback*

General Terms

Automatic, Measurement, Design

Keywords

Analog Design Automation, Operational Amplifiers, CAD tool

1. INTRODUCTION

In recent years, there is a high demand for fully differential circuits in high-frequency analog signal applications and multi-standard wireless receivers [3][1]. In general, fully differential circuits have a similar performance of DC gain, unity-gain bandwidth and power consumption, but twice of signal swing of their single-ended counter parts [2]. Fully differential amplifiers, compared with their corresponding single-ended, have a higher rejection capability, reduced distortion caused by harmonics, and larger dynamic range [11]. Also, common mode noise rejection represents a significant advantage of this kind of circuit [2]. These features make differential signaling a preferable choice for systems that require ADC's and differential transmission lines.

One common drawback of using fully differential amplifiers is that they need an extra circuit called common-mode feedback (CMFB) to maintain the amplifier stable. This circuit is used to establish the common-mode level - the average of the two outputs - at a desirable reference value, since a negative feedback results in a limitation of the common-mode component. Several topologies of CMFB circuits have been purposed for fully differential amplifiers [5][9][15]. Nevertheless, the specifications for an acceptable design are not clearly stated. As consequence, the design of an average CMFB circuit is evaluated by its qualitative performance. For example, the DC gain must be large enough to control the common-mode level with accuracy and the bandwidth must be higher than the main amplifier [8]. The traditional design of fully differential opamps is performed using an ideal CMFB circuit connected in the amplifier outputs. Then, the ideal characteristics of the CMFB circuit are used as the reference for the real circuit design, considering the qualitative constraints [7]. However, the method to satisfy these constraints are not clearly stated, so the designer have to find a way, which is not always the same, to find a solution.

While several computer-aid design (CAD) tools to specific design of high-performance fully differential amplifiers have been developed [17][16], many of them are based on methods that neglect the parameters used for designing the CMFB circuit or even the CMFB circuit itself. Tools based on the manually traditional method represents a good solution for the design of the fully-differential opamps [13], and show how CMFB circuitry can be critical on the design of this kind of circuit [17].

In this paper, we present a methodology for the design of fully differential operational amplifiers with CMFB using UCAF simulation-based automatic synthesis tool. Simulated-Annealing is used as optimization algorithm. The methodology is based on a two step process, where at first moment the fully differential amplifier is designed using an ideal CMFB circuit and, based on this result, the real CMFB is sized. We show that this methodology is very suitable for designing fully differential amplifiers with output balance.

The remaining of the paper is organized as follows: Section II presents the UCAF automatic sizing tool used to design the circuit; Section III presents the proposed methodology to design fully differential amplifiers with output balance; Section IV presents the results for the design of a fully differential amplifier; finally, Section V summarizes the main conclusions.

2. ANALOG INTEGRATED CIRCUIT SYNTHESIS TOOL

This work uses a simulation-based automatic synthesis tool called UCAF [14] to perform the design of fully-differential operational amplifiers. The tool uses an optimization heuristic, that can be either Simulated Annealing or Genetic Algorithms, to explore the design space and to find optimized solutions. The solutions are evaluated in terms of the constraints set, such as low-frequency gain and power dissipation. As inputs, the tool needs an initial solution that can be provided by the user or randomly, the specifications for the circuit, such as unity-gain bandwidth, slew-rate and others, and the technology parameters. The design specifications input also consider the range of variation of the transistor dimensions W and L (channel width and length, respectively), that are usually the limits of the input technology.

To evaluate the solution, the tool uses a multi-objective cost-function, as shown in Eq. 1. E_i represents the i^{th} specification that must be optimized, in a universe of n specifications. In this paper, the power dissipation is set as the minimization goal. E_j is the j^{th} constraint specification and $f(E_j)$ is the performance metric. This metric is directly dependent on the specifications that are maximum ou minimum constraints. The function is shown in Fig. 1. This function is dependent on the type of specification (minimum, as depicted in Fig. 2a, or maximum, as depicted in Fig 2b) and on the bounds of feasible and acceptable solutions a and b, respectively [4]. P_{Oi} and P_{Rj} are the weight parameters for each objective and constraint.

$$f_c = \sum_{i=1}^{n} P_{O_i}.E_i + \sum_{j=1}^{n} P_{R_j}.f(E_j) \quad (1)$$

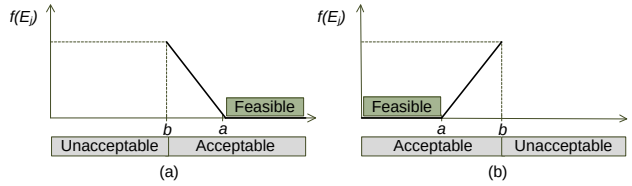

Figure 1: Cost function performance metric, (a) minimum required value specifications and (b) maximum required value specifications.

An important characteristic of this cost function is that non feasible solutions are admitted as possible circuit solutions during the optimization process. As shown in Fig. 1, unfeasible solutions have $f(E_j)$ values that depend on the distance between a required value and the measured specification value (E_j). It is done because a worst solution can be a path to a good solution in the design space exploration [12]. If these solutions are ignored, the algorithm can not explore this region effectively [10].

3. PROPOSED METHODOLOGY

This sections aims to present the proposed methodology to design fully differential amplifiers with output balance, i.e., considering the CMFB circuit as part of the design procedure. The method consists in a two step process, where the main amplifier is optimized first and then the feedback circuit is sized. A model for the fully differential amplifier using a CMFB circuit is shown in Fig. 2. The circuits of the model can be separate as main amplifier and CMFB blocks. The proposed design methodology divides the circuit in two parts in order to reduce the complexity of the circuit regarding the number of variables.

We use UCAF tool to design both main and CMFB amplifiers. In the first step, only the main amplifier is considered. The CMFB circuit is fixed as a high-level model. According to Fig. 2, the ideal CMFB circuit used to the first step is implemented by Eq. (2). Here, the constraint specifications are set in the tool by the user. Once the optimization process finds a solution that satisfy the design constraints and optimizes the objective function, the process is stopped. Then, the real CMFB circuit can be designed.

$$V_{cmc} = A_{cms}(V_{oc} - V_{cm}) + V_{bias} \quad (2)$$

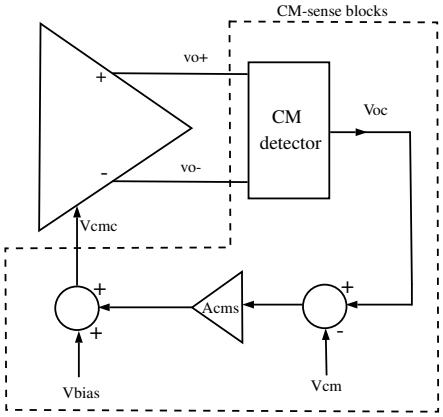

Figure 2: Conceptual Common-Mode Feedback block [6].

The design of CMFB circuit is made using the value of common-mode control voltage, V_{cmc}, of the main amplifier previously designed as design constraint. Once the output of the CMFB circuit is affected only by the common-mode voltage of the main circuit, it is possible to design the CMFB by keeping its output equal to the desired common-mode control voltage.

This design methodology is made in order to increase the compatibility between the main amplifier and the common-mode feedback circuit. Due this, an ideal model of CMFB is used and when the real circuit is designed its specifications should be closest to the ideal. With this, replacing the ideal model by the designed CMFB circuit, the specifications and the common-mode level control obtained for the ideal model should be kept.

4. RESULTS AND DISCUSSION

The proposed approach was validated with the design of a single-stage fully differential amplifier and the common-mode feedback circuit by using an optimization procedure to sizing the transistors. The following subsections show these results.

4.1 Single-stage Fully Differential Amplifier Design

This subsection describes the first step of the proposed approach, which is the design of a single-stage fully differential amplifier in XFAB 0.18 μm technology, using an ideal CMFB circuit. The schematic of the amplifier is shown in Fig. 3. The voltage sources V_{DD} and V_{SS} are set to 0.9 V and -0.9 V, respectively. The load capacitances, C_L, are fixed with a 10 pF value. In this amplifier, the common-mode control (CMC) input is the gate of the M_{5B} transistor. The CMFB loop gain should be high enough to force $V_{oc} \approx V_{cm}$ and the common-mode control to be approximately constant with $V_{cmc} \approx V_{bias}$. Both M_{5A} and M_{5B} transistors supply the tail current for the differential pair M_1-M_2. The V_{cmc} voltage is applied to provide the control of the common-mode (CM) level and designed to keep $I_{5A} = I_1 = |I_3|$ when the CM-level is equal to the desired reference V_{cm}. This implies that, in order to keep the circuit in correct operation and to provide the control of the CM-level, the CMC input should be $V_{cmc} = V_{bias} + \Delta V_{oc}$, with $V_{cm} = 0$.

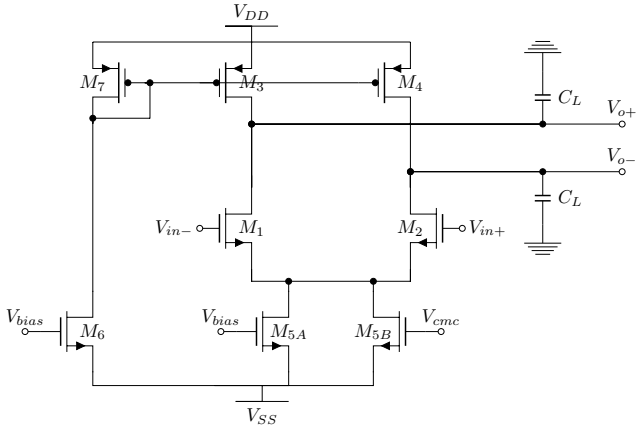

Figure 3: Schematics of a single-stage fully differential amplifier circuit.

The constraints for the design using an ideal CMFB are: the circuit specifications and the desired common-mode level (V_{cm}). The free variables used to explore the design space are the bias voltages and the transistor sizes for this circuit. This circuit have 7 free variables: W_1, L_1, W_3, L_3, W_5, L_5 and V_{bias}. In this design, Simulated Annealing is chosen as the algorithm to explore the design space. The specifications set as design constrains are the low frequency gain (A_{v0}), unity-gain bandwidth, phase margin (PM) and the slew-rate (SR). Minimization of power dissipation is the design objective. The results obtained for the specifications and the transistor sizes are shown in Table 1 and Table 2, respectively. The optimization procedure was executed in a Intel core i7 processor with eight physical cores and 8GB of memory. The result was achieved in 118 minutes.

4.2 Common-Mode Feedback Circuit Design

In the second step, the common-mode feedback circuit can be designed based on the main amplifier previously sized. Since $V_{cmc} = V_{bias} + \Delta V_{oc}$, this circuit must keep the DC output voltage at V_{bias} when the common-mode level is at the desired value. Also, based on the change of CM-level, its output should be influenced by only the output common-mode voltage. The CMFB circuit chosen to be designed is depicted in Fig. 4. The common-mode control voltage for the design of the main amplifier using an ideal CMFB circuit is about -167.045 mV. This value is a constraint for the optimization tool to design the real CMFB circuit. The obtained transistor values are shown on Table 3.

Table 1: Results obtained for the single-stage fully differential amplifier with an ideal CMFB.

Specifications	Required Value	Obtained Value
A_{v0} (dB)	$\geq$ 30.00	32.657
GBW (MHz)	$\geq$ 1.00	1.096
PM (^{o})	$\geq$ 50.00	91.29
SR (V/μs)	$\geq$ 1.50	3.8305
P_{diss} (μW)	Minimize	16.23
Run Time (min)	-	118

Table 2: Obtained transistor sizes for the fully differential single-stage amplifier.

Parameter	Obtained Value
W_1/L_1 (μm/μm)	36.29/19.70
W_3/L_3 (μm/μm)	27.41/6.83
W_5/L_5 (μm/μm)	15.30/9.75
V_{bias} (mV)	-167.045

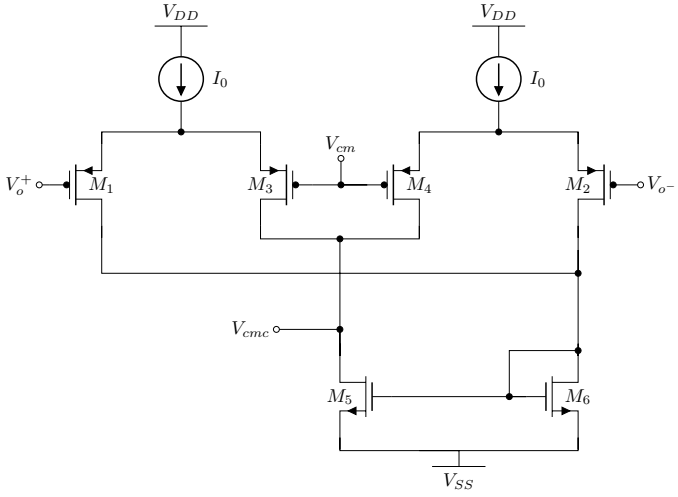

Figure 4: Common-mode Feedback Circuit.

4.3 Fully Differential Amplifier Results

With both, main amplifier and CMFB circuits sized, the ideal CMFB circuit used to design the main amplifier is replaced by the sized CMFB circuit. Table 4 presents the comparison between the results obtained by using an ideal

Table 3: Obtained transistor sizes for the common-mode feedback circuit.

Parameter	Obtained Value
W_1/L_1 (μm/μm)	35.91/89.18
W_5/L_5 (μm/μm)	7.19/46.28
I_0 (μA)	15.19

CFMB and the automatic designed CMFB. The results show that the obtained specifications using an ideal CMFB circuit were kept constant after the replacement of the real CMFB circuit.

Table 4: Comparison between the results obtained for the single-stage fully differential amplifier with an ideal CMFB and with the sized CMFB circuit.

Specifications	Required Value	Ideal CMFB	Sized CMFB
A_{v0} (dB)	$\geq$ 30.00	32.657	32.656
GBW (MHz)	$\geq$ 1.00	1.096	1.08
PM (^{o})	$\geq$ 50.00	91.29	88.63
SR (V/μs)	$\geq$ 1.50	3.8305	3.2
P_{diss} (μW)	Minimize	16.23	70.23
Run Time (min)	-	118	238

5. CONCLUSION

In this paper, a design methodology of fully differential amplifiers with output balance using an optimization based tool was proposed. The methodology was validated designing a 0.18 μm single-stage fully differential amplifier and its common-mode feedback circuit. The design of both circuits was divided in order to reduce the complexity in terms of circuits variables and design space. This design division allows us to satisfy the presented constraints for the amplifier, which was not possible using the hole circuit for the optimization process.

These results show that the methodology is very suitable to design fully differential amplifier with CMFB circuits. The power dissipation for the design of the common-mode feedback circuit was not a design constraint for the optimization process, which justify the increase of power after the replacement of the real CMFB circuit.

Other methodologies do not consider the design of the CMFB circuit for fully differential amplifier or even the CMFB itself, which turn the design of this kind of amplifiers too specific for an circuit topology. Our tool fill this gap, making the design of fully differential amplifiers using CMFB circuits less complex and general.

Acknowledgment

The grant provided by CNPq Brazilian research agency for supporting this work is gratefully acknowledged.

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