Temperature Fluctuation Effects on Performance of XOR Logic Gates

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ABSTRACT

This paper presents analysis and comparison between different transistor arrangements of XOR logic gates when temperature fluctuation is evaluated. The objective is to compare and verify timing characteristics, and identify which architectures are most appropriate to deal with temperature variation in the integrated circuit designs. Fourteen different XOR topologies were described in a predictive 32nm technology. The results show a range of performance variation from 40 % to 90 % according to the chosen transistor arrangement.

Keywords

XOR Logic Gate, Temperature Fluctuation, Performance, Nanotechnology.

1. INTRODUCTION

Exclusive-or function (XOR) is widely used in digital systems. Besides being present in most digital circuits, XORs are essential components in arithmetical circuits, comparators, parity generators and brokers/error detection, among others [1]. Consequently, the electrical characteristics of XOR logic gate are very important because they will significantly affect the final performance of such systems.

There are many different arrangements of transistors that can be used to implement the XOR function. Most proposed arrangements explore project concepts from two logic families: the traditional CMOS logic and the Pass Transistor Logic (PTL). The CMOS logic is the default logical style commonly used in the design of standard cell libraries. It explores the concept of complementary pull-up and pull-down planes. The PTL exploits the use of pass transistors. For various logic functions, the PTL style is capable of achieving an implementation with smaller area than CMOS logic [3]. However, the use of cascading PTL gates undertakes various electrical characteristics of the system. Many researchers propose topologies using a combination of the two approaches in order to exploit the best features of each strategy [1-3] [5-6] [10]. Facing great diversity of transistors arrangements that implement the XOR logical function, it becomes important to verify the behaviour of these different arrangements in the same testing framework for achieving a fair comparison.

The current systems are usually designed considering performance optimization. The temperature of system operation is directly connected with the circuit performance. When the temperature increases, the transistor drain current decreases, causing intuitively system performance degradation. Therefore, the influence of temperature variation in system performance must be verified and alternatives to mitigate this degradation investigated.

This article focuses on this context, evaluating several XOR logic gates in the same conditions, exploring the temperature fluctuation effects on propagation delay.

The rest of the paper is organized as follows. Section II presents a brief concept of temperature fluctuation. Section III presents the evaluated topologies of XOR logic gates. The methodology presented in Section III explores the description of circuits and simulation conditions. The results are discussed in Section IV. Finally, Section V presents conclusions.

2. TEMPERATURE FLUCTUATION EFFECTS ON MOSFET

Nanometric circuits are much more sensitive to variations in process (P), voltage (V) and temperature (T). The MOSFET current characteristics at different temperatures are analysed in [15]. Both device and interconnect performance have temperature dependence, with higher temperature causing performance degradation. Additionally, temperature variation across communicating blocks on the same chip may cause performance mismatches, which may lead to logic or functional failures. The net consequence of the temperature variation manifests itself on chip frequency variation [16].

As the temperature increases, the transistor drain current decreases. The junction temperature (the temperature at the semiconductor junctions forming the transistors) may significantly exceed the maximum ambient temperature. Commonly commercial parts are verified to operate with junction temperatures up to 125 °C. In Figure 1 is showed that the execution core has hot spots exceeding 120 °C, while the caches in the periphery are below 70 °C [8].

Conversely, circuit performance can be improved by cooling. Most systems use natural convection or fans in conjunction with heat sinks, but water cooling, thin-film refrigerators, or even liquid nitrogen can increase performance if the cost is justified. There are many advantages of operating at low temperature. As example, the subthreshold leakage is exponentially dependent on temperature. The aging effect BTI (Bias Temperature Instability) also has its degradation severity increased at high temperatures. [8].

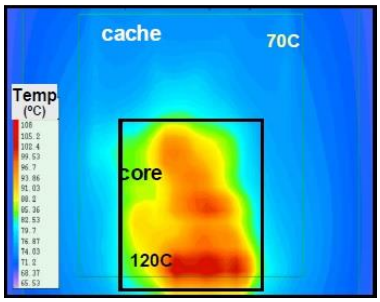


Figure 1. Thermal image of processor hot spots [16].

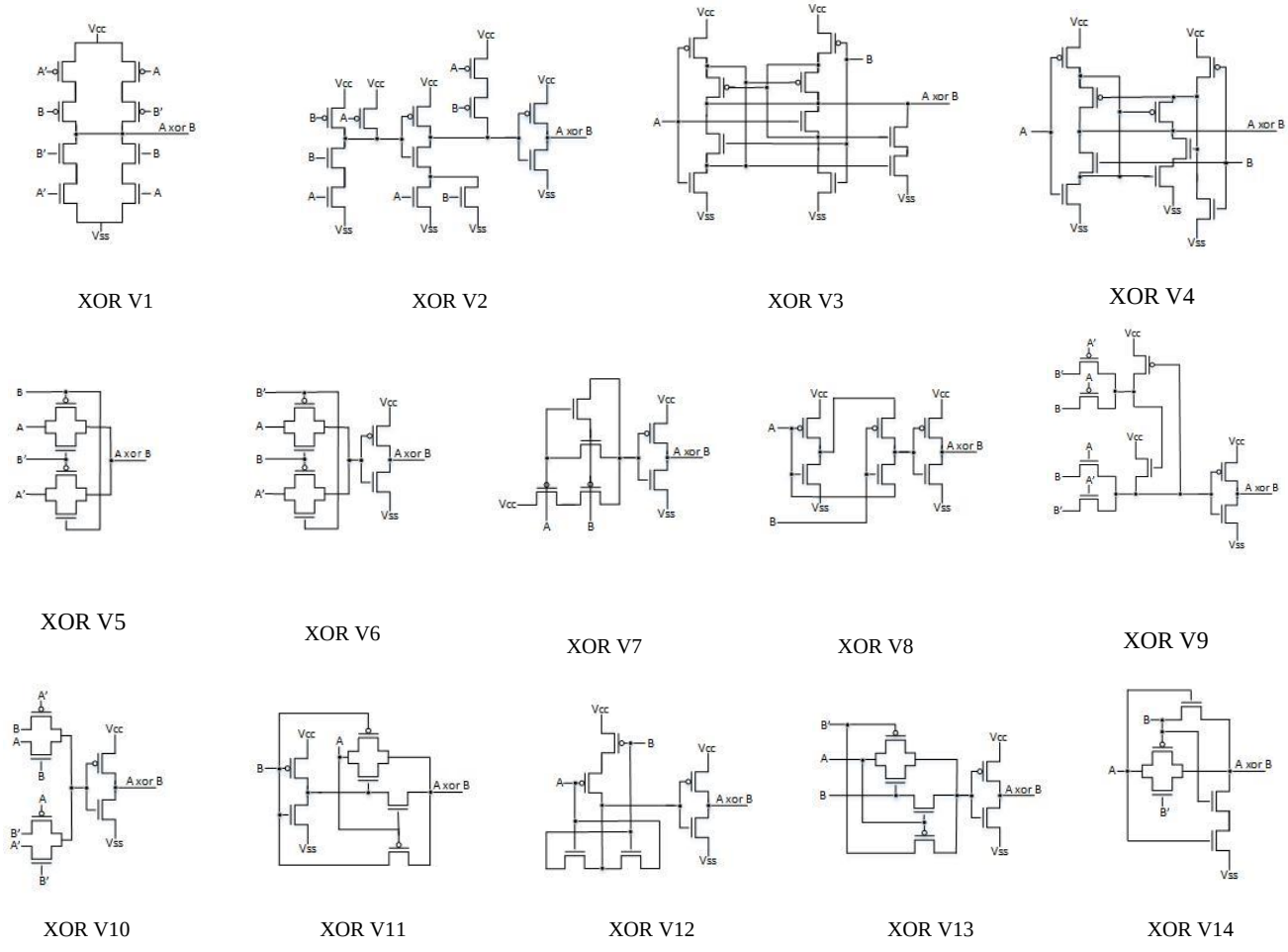
3. XOR LOGIC GATE

The exclusive-or function is generally known as a XOR logical operation between 'n' operands that results in a logical value true if and only if the number of operands with true values are unpaired. Commonly, it is represented by the symbol ⊕. Thus 'F = A ⊕ B' is a representation for an exclusive-or function of two inputs, A and B.

The XOR and XNOR functions have as their main feature act as a parity detector of logical operands, allowing comparison of input values. Different implementations of these functions may be obtained depending on how the transistors are arranged and the type of logic adopted. In this section different implementations of the XOR logic function that were explored in this work are presented in Figure 2.

The first row of Figure 2 illustrates four implementations of XOR gates that exploit the characteristics of CMOS logic family (V1 - V4) [5-8]. It contains complementary pull-up and pull-down networks. Their main feature is the high capability to drive the output signal. The input signals are only connected to the transistors gate terminal, isolating the output from the inputs. In other words, the output is being supplied exclusively by the power source of its own block. Thus, all arrangements tend to exhibit high robustness in case of noise [9].

The logic gates illustrated in the remainder of Figure 2 are the ones that exploit the concept of pass transistor (V5 - V14). The main difference from CMOS logic is that the input signals not only have the function of supplying the gate terminals but can also supply the output node through the pass transistors [1-8, 10]. Due to the characteristics of the XOR logic function, this aspect tends to reduce the number of transistors and the power consumption of these solutions. However, their output signals tend to be more



…ıe input [9].

Figure 2. XOR Logic Gates Arrangements

4. METHODOLOGY

This study evaluates 14 implementations of XOR functions under temperature fluctuation. All circuits were described as SPICE netlist and simulated electrically with NGSPICE. The predictive 32nm technology HP (high-performance) was used to describe the circuits [13].

All transistors were sized with channel length L = 32 nm and channel width of NMOS transistors Wn = 100 nm, and PMOS Wp = 200 nm. The supply voltage adopted is 1V. Two inverters are used in the input signal in order to emulate a more realistic signal [7]. Four inverters (Fanout 4) are used as load for each logical XOR gate. This structure is illustrated in Figure 3.

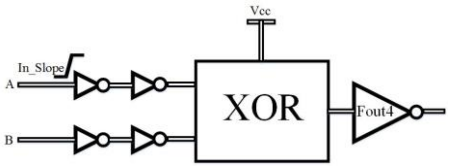


Figure 3. Circuit Evaluation Structure

The experiment consists of two steps. The first is the logic validation, which will confirm that all topologies will work properly. The second step consists in extracting delay data for all XOR gates. This work analyses the impact on gate delay when variations in the temperature of MOS transistors are applied. The temperature was varied from 25ºC to 125ºC and propagation delay for all timing arcs was taken for each temperature. The mean (μ) propagation delay, as well as the respective standard deviation (σ) of the experiments for all logic gates were compared. The relation between these values is emphasized through the normalized standard deviation (σ/μ), which allows a fair comparison of arrangements with different mean delay results.

4.1 Calculation of Delay

The propagation delay is the maximum time from the input crossing 50% to the output crossing 50% of nominal voltage, as show in Figure 4. The propagation delays are measured for all timing arcs of the XOR logic function. The average gate delay is computed and used to compare the performance results of different topologies. The standard deviation and the maximum delay are also evaluated.

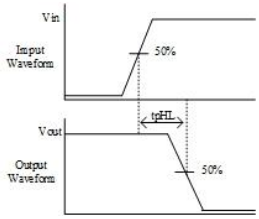


Figure 4. t_{pHL} Propagation Delay

5. RESULTS

The simulation results for each XOR are shown in Table 1. In the first column are described the evaluated logic gates ordered in the same manner that shown in Figure 2. In the next columns the values for mean and standard deviation of average delay time as well as the maximum delay time of the logic gates are shown. Since the objective of the work is to evaluate the robustness of the XOR topologies against temperature variation, the values presented in Table 1 are not the absolute delay, but the normalized delay. The use of the normalized values instead of the absolute values will simplify and provide a more fair analysis between the different topologies.

In terms of mean performance, the temperature fluctuation in relation of delay, XOR V9, XOR V10 and XOR V13 were more robust than the others, with about 65% variation between the highest and lowest delay. The gates XOR V1, XOR V7 and XOR V12 highlights were among those who had greater variation, with about 85% of deviation. The average delay variation versus temperature variation is also illustrated in Figure 5. From Figure 5 is possible to verify linear delay degradation as the temperature increases. The degradation slope can be considered the main difference between the lines, achieving a difference up to 40% in extreme cases.

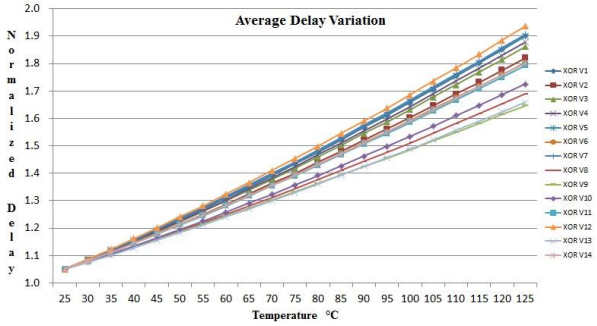


Figure 5. Average Delay Variation

The average delay data itself may mask relevant information. The standard deviation is the information that completes the delay behaviour. In standard deviation analysis three points should be highlighted. The first is illustrated in Figure 6 through XOR V8. In this situation, the standard deviation of average delay does not change with the temperature. The second is illustrated with dashed lines (XOR V7 and XOR V13) in Figure 6. In this case, the standard deviation is smaller in XOR V7 at 25 ºC and in XOR V13 at 125 ºC. This data shows that the standard deviation may vary differently according to the transistor arrangement. Finally, the solid lines in Figure 6 illustrate the higher severity caused by the temperature in standard deviation data.

The last analysis investigates the maximum delay variation according to temperature fluctuation. XOR V8 and XOR V13 highlighted with dotted lines in Figure 7, were more robust than the others, with about 40% maximum delay variation between the highest and lowest evaluated temperature. Among those who had greater variation, XOR V1 and XOR V4 stood out, with about 90% of variation, as can be observed in Figure 7, which exemplifies the temperature fluctuation in relation to the delay. When compared to the average delay variation, the maximum delay presents a higher degradation slope difference between the topologies. In maximum delay, this difference is more than 100%.

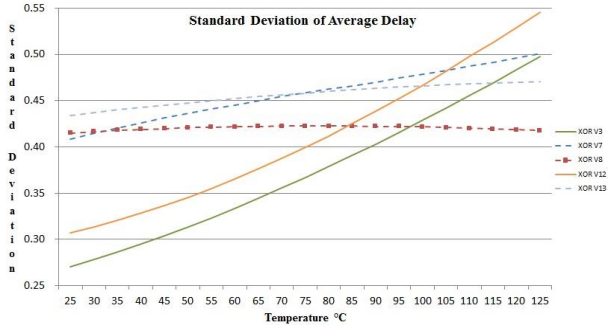


Figure 6. Standard Deviation of Average Delay

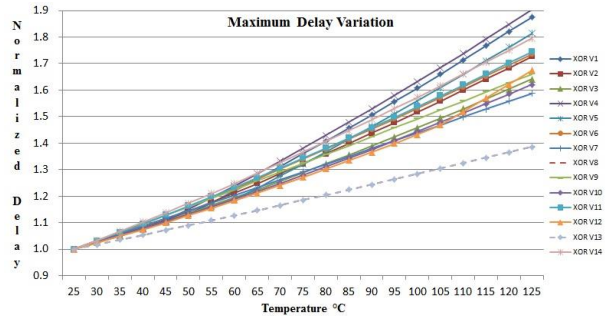


Figure 7. Maximum Delay Variation

6. CONCLUSION

A comparison of a large number of XOR cells was performed in this study. As expected, the increase in temperature directly affects the driving of loads, making considerably increase on the delay of the gates. Considering the different conditions that the integrated circuits are submitted, the results presented in this work provide valuable data to be used in design of more robust circuits, such as adders formed from intermediate blocks composed primarily of XOR logic gates [13][14].

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Table 1. Normalized Timing Results under Temperature Fluctuation

XOR	μ					σ					Maximum Delay				
	Temperature ºC					*Temperature ºC*					*Temperature ºC*				
	25	**50**	**75**	**100**	**125**	**25**	**50**	**75**	**100**	**125**	**25**	**50**	**75**	**100**	**125**
V1	1.00	1.18	1.38	1.61	1.85	0.16	0.19	0.23	0.27	0.33	1.00	1.13	1.36	1.61	1.88
V2	1.00	1.17	1.35	1.55	1.77	0.07	0.06	0.06	0.07	0.08	1.00	1.14	1.32	1.52	1.73
V3	1.00	1.17	1.37	1.58	1.81	0.27	0.31	0.37	0.43	0.50	1.00	1.13	1.29	1.46	1.64
V4	1.00	1.18	1.38	1.59	1.83	0.19	0.23	0.28	0.34	0.41	1.00	1.15	1.38	1.63	1.90
V5	1.00	1.18	1.39	1.61	1.85	0.16	0.18	0.21	0.26	0.30	1.00	1.13	1.32	1.56	1.81
V6	1.00	1.16	1.34	1.54	1.75	0.12	0.13	0.15	0.16	0.18	1.00	1.16	1.34	1.53	1.74
V7	1.00	1.19	1.39	1.62	1.86	0.41	0.44	0.46	0.48	0.50	1.00	1.14	1.29	1.44	1.59
V8	1.00	1.14	1.29	1.46	1.64	0.42	0.42	0.42	0.42	0.42	1.00	1.09	1.19	1.28	1.39
V9	1.00	1.14	1.28	1.44	1.60	0.49	0.55	0.60	0.66	0.71	1.00	1.16	1.32	1.49	1.66
V10	1.00	1.14	1.31	1.48	1.67	0.14	0.15	0.16	0.17	0.18	1.00	1.13	1.28	1.44	1.62
V11	1.00	1.16	1.34	1.54	1.74	0.10	0.11	0.13	0.15	0.16	1.00	1.16	1.34	1.54	1.74
V12	1.00	1.19	1.40	1.64	1.89	0.31	0.35	0.40	0.47	0.55	1.00	1.13	1.27	1.43	1.67
V13	1.00	1.13	1.28	1.44	1.61	0.43	0.45	0.46	0.47	0.47	1.00	1.09	1.19	1.28	1.39
V14	1.00	1.16	1.34	1.54	1.75	0.16	0.19	0.22	0.25	0.29	1.00	1.17	1.36	1.57	1.79