Optimization of gated lateral PIN photodiodes

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ABSTRACT
Based on bidimensional numerical simulations (fulfilled through the Atlas software) and the semiconductor-device structure, we analyze the operation principles of gated Lateral PIN (LPIN) photodetectors, including carriers concentration, recombination rate and current–voltage characteristics in order to check the influence of the gate size, placement and bias. Six different configurations for different wavelengths and gate materials were tested. The best performance in terms of current level was presented by the device with no gate, however, it showed no carriers control on the oxide-semiconductor interface. On the other hand, the carriers control obtained by the full gate device was high, but the current level was really low. In order to overcome this compromise between current level and carrier's control, we propose a new configuration of lateral photodiode, the dual gate device, which can provide a satisfactory result in terms of current level and carrier's control.

Keywords
Photodiodes; gate; PIN; recombination rate; carriers concentration.
General Term
Measurement, Performance, Design, Experimentation, Verification, Theory.

1. INTRODUCTION

Semiconductor devices have played an essential role in microelectronics nowadays. In this scenario, silicon optoeletronic devices are widely used since the light penetration can generate electron-hole pairs, which if separated will contribute to the photocurrent. The level of the generated current will be proportional to the energy of the incident photons, that depends on their wavelength, thereby conversion of light signals into electrical signals is made [1].

One of the most common photosensors is the PIN photodiode. This device consists of a PN junction separated by an intrinsic region with length L_I, which, in practice, corresponds to a weakly doped P or N region. The phenomena that occur in the intrinsic region are very important, since they can change the characteristics of the depletion layer and hence the collected photogenerated carriers. Therefore, the operation of the device is related to the characteristics of the photodiode such as intrinsic region length, P+ and N+ regions length and the total length. All these quantities will dictate the size of the photosensitive area, and, in practical terms, the larger the photosensitive area, the higher the device current [2].

In Lateral PIN photodiode devices, unlike the conventional vertical photodiodes, a depletion region can be formed really next to the surface. This fact is very important, because the depletion region has a lower recombination rate, once the carriers photogenerated inside this region are separated more efficiently due to the high electric field, especially for lower wavelengths [3].

In general, gated PIN photodiodes have very attractive features for optical devices. The gate voltage (V_G) can change the operation mode of the intrinsic region due to the charges induced on the substrate, by promoting accumulation, depletion or inversion. This work aims to optimize this process through a thorough study using numerical simulation. The goal is to estimate the best relative gate placement, as well as, the best gate length in order to improve the device performance. In contrast, the presence of the gate can mean a reduction of the photosensitive area, because, in fact, it is an obstacle in the path of light incidence, since most of the gate currently used materials have high reflectance index (55%~90%) [4]. Furthermore, concerning the gate design (length and placement), the gated photodiode has a trade-off between depletion region thickness increase and photosensitive area decrease.

2. DEVICE CHARACTERISTICS

The characterized devices were simulated using the 0.25µm ON-Semiconductor Technology described in [5], which are showed in Table 1. All the parameters were based on [6]. A cross-section of one finger of the device can be seen in Figure 1.

Table 1. Parameters of Lateral PIN diodes

Parameters	
P and N region width (L_P and L_N)	6.5 µm
Intrinsic region width (L_I)	11 µm
Oxide layer thickness (T_{ox})	13.8 nm
Junctions thickness (T_P,T_N)	0.15 µm
Intrinsic region doping concentration (N_I)	$6x10^{16}cm^{-3}$
P region doping concentration (N_{P+})	$1x10^{19}cm^{-3}$
N region doping concentration (N_{N+})	$1x10^{20}cm^{-3}$

Six types of devices were simulated. The first one can be seen in Figure 2-A. It has a left offset gate, which is placed adjacent to the P+ region. In the same way, Figure 2-B and Figure 2-C represent the right offset gate device and the central gate device respectively. Figure 2-D shows de dual gate device, which has two gates adjacent to the P+ and N+ regions, with a region with no gate in the middle. A typical gated lateral photodiode can be seen in Figure 2-E where the gate is over the entire intrinsic length. In order to make the comparisons, a no gate device was simulated as well (see Figure 2-F). These six variants of gated lateral p–i–n junction devices were simulated in order to study the difference in operational behavior due to relative gate placement and its bias.

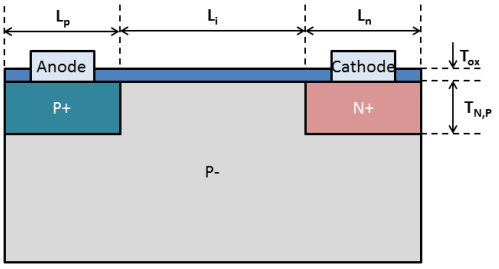

Figure 1. Cross-section of one finger of a PIN photodiode.

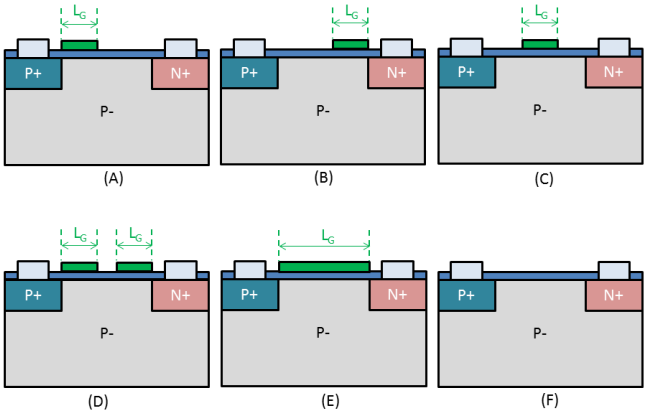

Figure 2. (A) Offset left: device with the gate adjacent to P+ region. (B) Offset right: device with gate adjacent to N+ region. (C) Central gate: gate in the middle of the device. (D) Dual gate: device with simultaneous right gate and left gate . (E) Full gate: gate all over the entire intrinsic region. (F) No gate: common lateral PIN photodiode, with no gate.

3. DISCUSSION

As the devices described here have the architectural characteristics of both p–i–n diodes and MOS field-effect transistors so we performed measurements looking into the behavior of these devices from both an electrical and an optical perspective. The best way of looking at these hybrid devices operationally is to consider them as gated diodes. The current–voltage characteristics are then interpreted as the reverse-biased characteristics of a junction diode but with the added control on current exercised by the MOS gate. In this paper we set out the details of both electrical and optical measurements carried out on the six device variants.

There are 3 parameters of the device (proposed in this work) that are directly related to the current: the gate length, bias and position.

The gate length determines the device fill factor (ratio between photosensitive area and the total device area) because it is a barrier to the incidence light. The greater gate length, results in a smaller photosensitive area, thus the lower the current flowing in the photodiode.

The gate voltage (V_G) determines the mode of operation of the first interface. Positive gate voltage promotes depletion below the gate (and perhaps inversion), while negative gate voltage promotes accumulation.

Depending on the gate placement, its most interesting bias could change, because it would affect the intrinsic region in a different way due to change in carrier's concentration. To make this issue more clear, Figure 3 shows the carriers concentration of four different structures, all of them with gate length (L_G) of 9µm and total length of 24µm.

It is more convenient to analyze the concentration of holes when negative V_G is applied (since it induces the accumulation of positive charges in the first interface), and the depletion when V_G is positive, in which inversion can be achieved. Therefore the structures in Figure 3 were plotted considering the concentration of carriers (electrons for $V_G > 0$, and holes for $V_G < 0$), covering the region from 0.02µm to 0.2µm on y axis and 0µm to 24µm on the x axis of the devices. Towards achieve real feature simulation, the following models were used: "kla", "fldmob", "bgn", "watt", "klaaug", "consrh" and "optr".

Figure 3-B shows the hole concentration of the offset left device with negative V_G, since it causes accumulation of holes underneath the region adjacent to the p-contact. This had the effect of extending the p contact, reducing the distance between the two electrodes. [7].

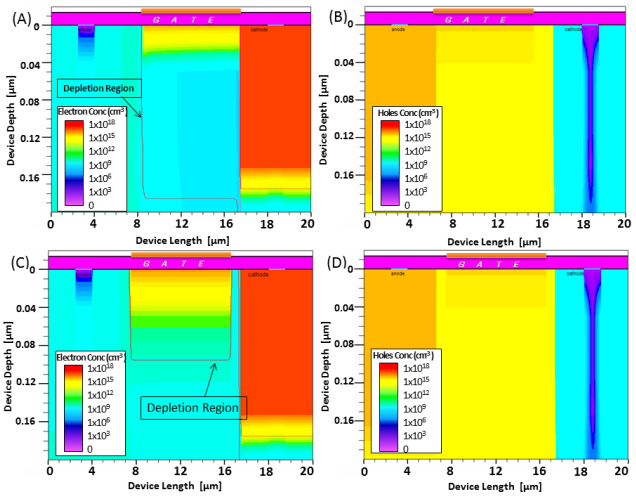

Figure 3. Cross-section of a photodiode structure showing electrons concentration for positive V_G, and holes concentration for negative V_G for (A) Offset right device with V_G=+3V. (B) Offset left device with V_G=-3V. (C) Central gate device with V_G=+3V. (D) Central gate with V_G=-3V. All the structures are under light incidence of wavelength (λ) of 637nm.

When comparing Figure 3-A and Figure 3-C, one can note that the size of depletion region of the offset right device is larger than the one presented by the central gate. This occurs because the depletion region formed under the gate in Figure 3-A merges to the depletion region formed by the intrinsic region and the N+ region (junction depletion region). This is a very important issue of this device, since the depletion region shall have then 9µm of length rather than 0.01µm, when there is no gate on the device (this result can be obtained using equation (1)), this is equivalent to increase the depletion region in 900 times.

$$d = \sqrt{\frac{2\varepsilon_{SI}(V_{BI}-V_D)}{q}\left(\frac{1}{N_I}+\frac{1}{N_{N+}}\right)} \quad (1)$$

Where, ε_{SI} is the silicon permittivity, V_D is the anode bias, q is the elementary charge and V_{BI} is the built-in potential given by:

$$V_{BI} = \frac{KT}{q}\ln\left(\frac{N_I N_{N+}}{{n_i}^2}\right) \quad (2)$$

Where, $\frac{KT}{q}$ is the thermal energy and n_i is the intrinsic concentration of carriers [8].

On the other hand, the central gate (Figure 3-C) showed a smaller depletion region for the same gate voltage, besides being a discontinuous depletion region, that may have strong influence of recombination phenomena. Figure 3-D shows the central gate device with negative gate bias. It is possible to observe that there is a decrease in the electron concentration in a region below the first interface, that is similar to the one presented by the offset left device (Figure 3-B). To better understand the functionality of each device, there were made plots of the photogenerated current (I_{TOTAL}) as a function of the gate voltage (V_G), for anode bias (V_{ANODE}) of -1.5V that can be seen in Figure 4. For this curves, the considered wavelength was 637nm, which corresponds to the red light and the incidence power light (P_{IN}) was $1x10^{-3}$ W/cm^2. It can be seen that the higher current was presented by the device with no gate, represented by the continuous line, due to the higher photosensitive area. The other three devices (central gate, offset right and offset left) presented lower photogenerated current than the device with no

gate independently of the gate length, mainly due to the presence of a high reflective material on top of the intrinsic region (we considered the aluminum as gate material).

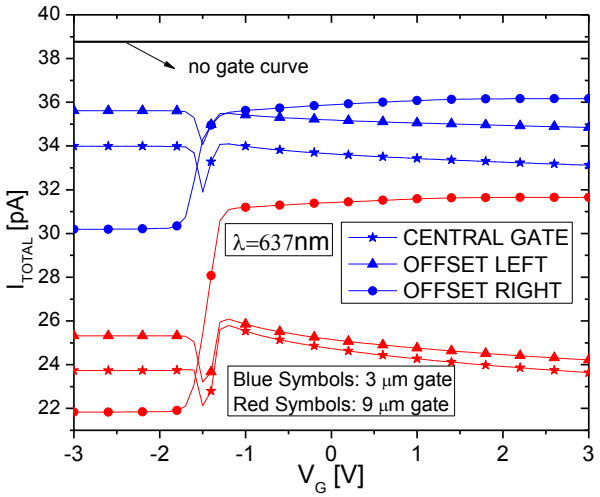

Figure 4. Photogenerated current (I_{TOTAL}) as a function of the gate bias (V_G) for different devices, for two gate lengths, under the light incidence of 637nm.

When the gate voltage is changed, the operation modes of the devices are changed as well, and this explains the behavior of the current levels when pushing the intrinsic region in accumulation (negative V_G) or inversion (positive V_G). When the intrinsic region is pushed in depletion mode (around -1.5V of V_G), the current abruptly decreases, independently of the gate length. For V_G smaller than -2V, the higher current level was presented by the offset left device (for both gate lengths), while for V_G greater than -1V, the higher current was presented by the offset right device. The facts mentioned before can be explained as follows: in the case of V_G<-2V, accumulation is promoted under the gate, and when this happens in the offset left device, it has the effect of extending the p contact, reducing the distance between the two electrodes, decreasing the probability of carries recombination in intrinsic region and thus increasing the current. On the other hand, for V_G>-1V, the offset right device promotes a huge continuously extension of the depletion layer formed between the N+ and the intrinsic region, producing a reduction in the recombination rate, that increases the photogenerated current. The central gate device does not present any interesting feature concerning to the photogenerated current and showed intermediate current levels for the two gate lengths. So far, it was demonstrated that the offset left device has interesting properties when polarizing the device in accumulation mode, though, the offset right device showed to have interesting results when the device is working in depletion (or even inversion mode). However, both of them presented lower current levels than the device with no gate. In this way, we performed simulations with a different gate material called ITO (Indium Tin Oxide) that shows a very low reflection index and can be considered transparent to visible light [9]. For these simulations, a work-function of 4.5eV was considered [10] and the total diode current as a function of V_G is shown in Figure 5 for the central gate, offset right and offset left devices for L_G=3μm and 9 μm. As can be seen, for V_G>-2V, the offset right gate device presented a higher current than that in which the device with no gate (black continuous line) was used. This is because the "invisible" gate overcomes the problem of the reflection of the incident light that occurs when using metal gates, leaving only the beneficial influence of the gate (the larger depletion layer). The ideal device would be the one that has the invisible gate (ITO) over the entire intrinsic region, that is shown by the dashed lines in Figure 5 and it is a result from the fact that this device has a depletion region through the entire device channel [11].

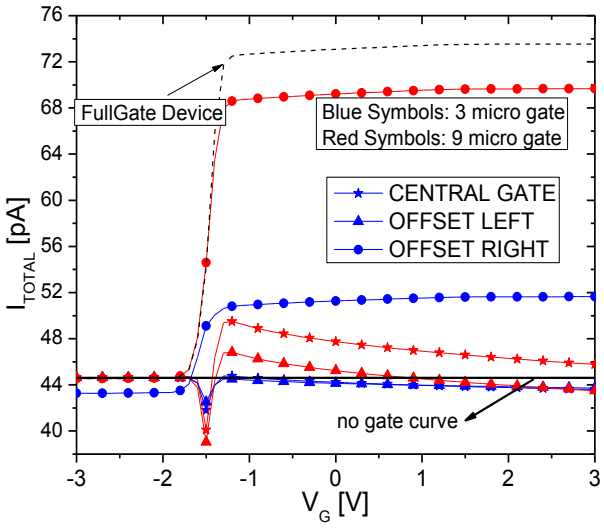

Figure 5. Photogenerated current (I_{TOTAL}) as a function of the gate bias (V_G), for different devices and gate sizes, with the ITO gate material for λ of 637nm.

As the offset right gate device shows interesting features in depletion mode, Figure 6 shows the diode current for four different gate lengths made in aluminum, in order to compare the effect of the gate length variation on the performance of this device. As the gate length is decreased from 9μm to 1.5μm, the current increases in around 37%. However, independently of the gate length, the devices presented lower currents levels than that presented by the device with no gate, because the negative effect of the reduced photosensitive area predominates over the depletion region increase.

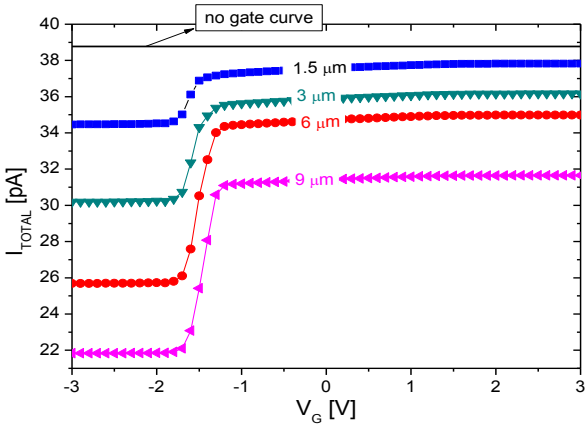

Figure 6. Photogenerated current as a function of the gate voltage (V_G) for the offset right device with different gate lenghts. (with gate material of aluminum) for λ of 637nm.

From the results of the previous analysis, it can be concluded that higher current levels are able to be achieved in two situations: when the right offset gate had a positive gate voltage and when the left offset gate had a negative bias. Therefore, one important purpose of this paper is the dual gate device (that is shown in Figure 2-D). This device has two gates adjacent to the P+ and N+ regions, with a region with no gate in the middle. By taking advantage of the difference in the gate voltage effect on the

intrinsic region, depending on the gate placement, this device can be considered very interesting in terms of current level increase.

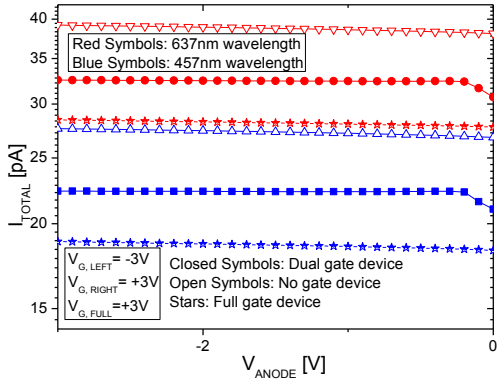

Figure 7. Photogenerated current as a function of the anode bias for dual gate ($V_{G, LEFT}$=-3V and $V_{G, RIGHT}$=+3V), full gate ($V_{G, FULL}$=+3V) and no gate device with aluminum gate material.

Figure 7 shows the total diode current as a function of the anode voltage for three types of devices: the dual gate, the full gate and no gate device with aluminum gate. As can be seen, the full gate device shows the lower current owing to the reduced photosensitive region and consequently smaller fill factor. On the other hand, when the device has no gate, the current level is the highest one, but this device does not offer any control of the charges in the oxide-semiconductor interface. This trade-off between photosensitive area and charges control can be overcome by using the dual gate device, that presented intermediate level of current due to the presence of a larger photosensitive area than the full gate device, as well as, a reasonable charge control. All in all, when the gate contact material is the ITO, the dual gate device has a current lower than the full gate device, so the best choice in this case (ITO metal contact) is the full gate.

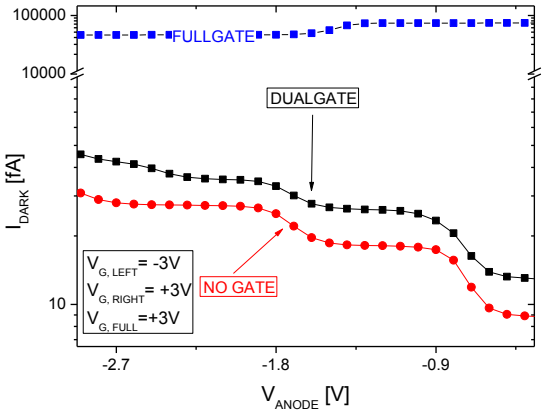

Figure 8. Dark current (I_{DARK}) as a function of the anode bias for dual gate and no gate devices for ITO gate material.

One important figure of merit of photodetectors is the dark current, shown in Figure 8 as a function of the anode voltage. The dark current is the current presented by the device with no light incidence, and is especially due to thermal generation of carriers. It can be seen that the full gate device has higher current level, owing to the larger depletion region where the carriers generated by thermal agitation are more likely to recombine. Besides, when the device has no gate, it shows a lower dark current, while the dual gate, has intermediate dark current level, just similar to the behavior with light incidence. This advantage of the dual gate device can be more clearly seen in Figure 9, where it is observed the recombination rate of the intrinsic region as a function of the device length. The ideal situation is achieved when the recombination rate tends to zero.It can be seen that the recombination rate is reduced especially in the regions below the gate, both for the case of the dual gate and the full gate device. Therefore, the lowest recombination rate happens in the full gate device, in which the depletion region is formed all along the intrinsic region.

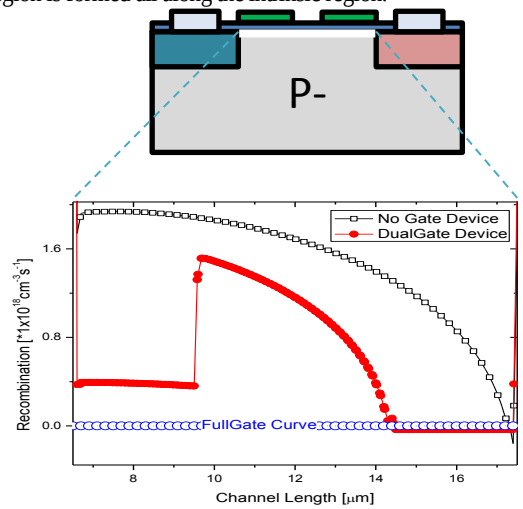

Figure 9. Recombination rate as a function of the device length. This plot was made considering a cross-section of the first interface through the channel.

4. Conclusions

In this work the operation of lateral gated photodiodes regarding gate size, placement and bias was analyzed. In order to account for all the effects of these parameters, six different configurations were tested. In the case of aluminum gate material, the best choice in terms of current level was presented by the lateral photodiode with no gate, however, when the carriers control is considered, the full gate device showed to be the best choice. In order to overcome this trade-off, we proposed a device that actually has two gates, called the dual gate device. It has one gate positioned adjacent to the P region, and a second gate positioned adjacent to the N region. In addition to presenting satisfactory performance in terms of responsivity and electrostatic control, the dual gate device is fully compatible with the fabrication processes of integrated devices.

5. References

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