Envelope Tracking Power Amplifier in CMOS Technology for 4G LTE Wireless Communication Systems Handsets

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ABSTRACT
The high efficiency and linearity required by 4G LTE wireless communication standard poses several challenges, notably for transmitter design. To overcome these challenges more efficient topologies for power amplifier (PA) networks, such as Envelope Tracking (ET), that can handle linear constituent PAs are being used. CMOS technology is the choice for cheaper devices. This work study the different blocks of an ET amplification network, designing and analyzing the behavior of an envelope amplifier and RF PA integrated on such a system.

Keywords
CMOS technology, envelope tracking, power amplifier, radio-frequency, wireless communication systems.

1. INTRODUCTION
During the past few years, the telecommunication sector has undergone rapid evolution. The first wireless communication systems were only able to transfer voice data. However, recent technologies allow the transmission of not only voice data, but also images and video. The fourth generation (4G) or Long Term Evolution (LTE) transmission standard technology currently being implemented offers not only high spectral efficiency but also high data rate transmission [1]. To this end, 4G technologies use orthogonal frequency-division multiple access (OFDMA), which increases the peak-to-average power ratio (PAPR) of the modulated signal that is being transmitted.

The 4G LTE wireless standard also requires highly linear transmitters, which poses a challenge for the design of the RF power amplifiers (RF PA) that are responsible for amplifying the input signal power [2]. Highly linear RF PAs are not as efficient because they consist mainly of power transistors [3].

Therefore, the average efficiency of an RF PA, used to amplify high PAPR signals, is very low, resulting in reduced battery autonomy for handsets and greater costs related to heat dissipation in RF base stations.

To overcome these design challenges, different amplifying architectures that can enhance efficiency have been developed. The most promising one is the "Envelope Tracking" which allows supply voltage control, enabling the circuit to operate with constant efficiency over a wide range of input power levels.

The development of CMOS technology has also played a big part in the evolution of the telecommunication sector. CMOS provides small components that can easily be integrated as one circuit. Although digital circuits have benefitted from scale reduction, analog circuits - and specially RF PAs - still have a lot of challenges to overcome before they can be totally integrated using CMOS technology. This is due to the fact that CMOS systems require a low breakdown voltage, forcing the RF PAs to operate under small supply voltages. To develop the high level of output power demanded by 4G LTE handsets, devices must be able to handle high currents. This in turn increases the losses associated with heat dissipation, compromising the overall efficiency of the circuit. CMOS also suffers from lossy substrate [4].

In order to understand the challenges of the RF PA design, considering the limitations previously discussed, this work presents a study of an amplification network, implemented using CMOS technology, which uses the ET topology for 4G LTE wireless communication applications.

This article is organized as follows. Section 2 describes a traditional linear amplifier and Section 3 presents the ET topology. Sections 4 and 5 discuss specific design topics related to each main blocks of an ET amplification network. Section 6 contains the results from computer simulations of the aforementioned PA network. Finally, conclusions are summarized in Section 7.

2. CLASS B POWER AMPLIFIER
Power amplifiers are devices composed of power transistors, whose purpose is to amplify the power of a signal. In order to satisfy the needs of the different applications in which RF PAs are found, power transistors can work in different classes of operation that can be split into linear (class A, B and AB) and non-linear (C, D, E and F) [3].

The 4G LTE wireless communication network requires highly efficient and linear transmission systems, this work therefore concentrates on class B RF PAs.

An idealized example of a class B RF PA schematic is shown in Figure 1. This kind of amplifier is known as a push-pull amplifier because it consists of two complementary transistors, one NMOS and one PMOS. The first one operates during the positive half cycle of the input signal, pushing current to the load, while the later one operates during the negative half cycle of the input signal, pulling current from the load.

For the present circuit analysis we use an idealized piecewise linear model for the transistors. It is assumed that the gate current is always zero for both transistors, while the drain current response changes according to the operation mode of the transistor. When the transistor is cut-off, the drain current is zero

($v_{GS} < 0$ for NMOS and $v_{GS} > 0$ for PMOS). If the transistor is saturated ($v_{GS} \geq 0$ for NMOS and $v_{GS} \leq 0$ for PMOS) the drain current is proportional to the gate-source voltage ($i_{DS} = g_m v_{GS}$), where g_m is the transistor transconductive gain in saturation mode.

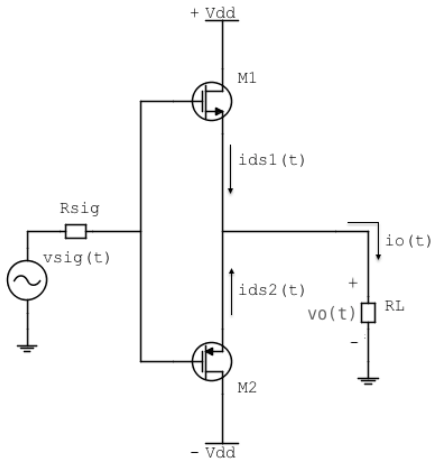

Figure 1 – Schematic of an idealized class B RF PA.

For class B RF PAs, the quiescent point is set between the saturation and the cut-off regions of its transistors which means that their DC bias voltage (v_{GS}) are equal to the threshold voltage (V_{th}, for an idealized circuit, $V_{th} = 0$). Considering that the circuit is piecewise linear, the analysis can be separated in two different situations.

The first case analysis, which is valid only for the positive half cycle of the input signal, assumes that M1 is saturated and M2 is cut-off. This leads to the following relations among the circuit currents and voltages (the current and voltages shown in the equations below are all defined in Figure 1):

$$i_{DS1}(t) = \frac{g_m}{1 + g_m R_L} v_{SIG}(t), \tag{1}$$

$$i_{DS2}(t) = 0, \tag{2}$$

$$v_{DS1}(t) = V_{DD} - g_m R_L v_{SIG}(t), \tag{3}$$

$$v_{DS2}(t) = V_{DD} + g_m R_L v_{SIG}(t). \tag{4}$$

The second case analysis, which is valid only for the negative half cycle of the input signal, it is assumed that M2 is saturated and M1 is cut-off. Redoing the first calculation, it is possible to prove that (3) and (4) remain the same, while (1) and (2) become:

$$i_{DS1}(t) = 0, \tag{5}$$

$$i_{DS2}(t) = \frac{g_m}{1 + g_m R_L} v_{SIG}(t), \tag{6}$$

As for the load, since there are two complementary transistors in this topology, the voltage on R_L will always be:

$$v_O(t) = \frac{g_m R_L}{1 + g_m R_L} v_{SIG}(t), \tag{7}$$

and the current that runs through R_L terminals will be given by:

$$i_O(t) = i_{DS1}(t) + i_{DS2}(t) = \frac{g_m}{1 + g_m R_L} v_{SIG}(t). \tag{8}$$

Considering the circuit input as a sinusoidal signal ($v_{SIG}(t) = V_{sig} \sin(\omega_0 t)$), it is possible to obtain the average efficiency of this RF PA. The average power on the load is given by:

$$P_{R_L} = \frac{V_0^2}{2R_L}, \tag{9}$$

where V_0 is the amplitude of the voltage on the load.

The current that runs through all DC supply voltages (V_{DD}) is the same as transistors' drain current, i.e. half-wave rectified waveforms. Hence, to find the DC levels of those currents, a Fourier transform is used. The sum of DC power delivered by all supply voltages is equal to:

$$P_{DC} = 2V_{DD} \frac{V_0}{\pi R_L}. \tag{10}$$

The ratio between (9), the power delivered to the load, and (10), the power developed by all DC voltage supplies, gives the circuit efficiency (η):

$$\eta = \frac{\pi V_0}{4V_{DD}}. \tag{11}$$

From (11) it is noticeable that the average efficiency of a class B amplifier is proportional to load voltage amplitude. Maximum efficiency (78.5%) is achieved only when $V_0 = V_{DD}$. However, due to the high PAPR of OFDMA signals, average efficiency will be significantly reduced.

3. ENVELOPE TRACKING TOPOLOGY

4G LTE technologies require transmission systems to be linear. However, the compromise between efficiency and linearity imposed by the RF PAs can make this process really challenging. Because of this, new amplification network architectures have been proposed. Among them all, the one that shows the biggest potential is the Envelope Tracking (ET) topology [4].

This architecture is based upon Kahn's Envelope Elimination and Restoration (EER) [3]. Although ET consists mainly of the same two elements as EER, an Envelope Amplifier (EA) and an RF PA, ET is able to control the RF PA supply voltage according

to the input signal envelope variation. Figure 2 presents a block diagram of the ET topology.

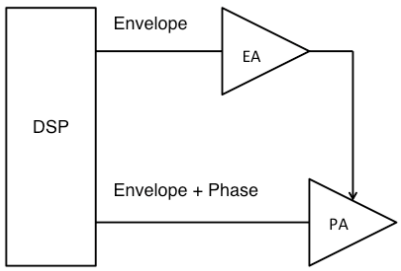

Figure 2 - Envelope Tracking amplification network schematic.

The RF PA amplifier of the ET amplification network is responsible for the linear amplification of the original RF signal, preserving the envelope and phase modulation information. The main purpose of the EA is to control the RF PA supply voltage according to any envelope variation of the input signal. By controlling the supply voltage of the RF PA it is possible to maintain the operation of this device at a constant efficiency, even if the signal to be amplified has a variable envelope.

If the ideal class B RF PA analyzed in Section 2 were to be integrated in an ET amplification network, for example, V_{DD} would always be equal to V_0, allowing this device efficiency to be constant and equal to the maximum value (78.5%) during the whole amplification process.

4. ENVELOPE AMPLIFIER

In an ET amplification network, the EA's only role is to modulate the RF PA supply voltages. The linearity and bandwidth constraints on the EA are, therefore, not very strong. The bandwidth usually just needs to be equal to the input signal bandwidth (a few MHz). Moreover, the energy of 4G LTE signals is mostly concentrated around the DC point.

The hybrid amplifier (HA) provides an efficient architecture for the EA [5]. In a HA topology, the amplification is shared between two amplifiers: one linear and one non-linear. The first one is implemented by an operational transconductance amplifier (OTA) given by a folded-cascode amplification stage followed by a rail-to-rail class AB stage. In the later one, the transistor works as a switch, usually resulting in a buck converter. A hysteresis controller does power distribution between amplifiers. In order to deliver the amplified signal with the best efficiency, this controller exploits the best characteristics of each amplifier: the non-linear amplifier handles low-frequency components, while the linear amplifier handles high-frequency components.

In this work, the efficiency of the linear amplifier (OTA) was investigated. Considering that the rail-to-rail class AB output stage plays a major role in determining the overall OTA efficiency, only this part of the circuit is implemented. The nonlinear amplifier is modeled as an ideal DC current source (I_{dc}) in parallel with the load R_2, as shown in Figure 3.

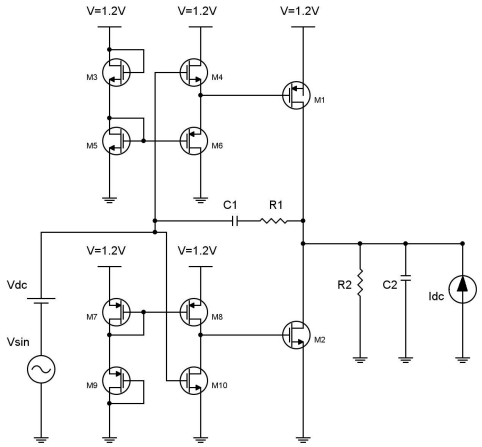

Figure 3 – Rail-to-rail class AB output stage of the linear OTA amplifier.

5. RF PA

Wireless communication development is directly related to electronics evolution. The advent of CMOS technology has allowed analog devices downscaling facilitating the complete integration of the circuits which led to cheaper devices. Thus digital circuits have taken advantage of the small size of CMOS technology, analog circuits have faced some design challenges. Among all analog circuits inside a wireless transmitter, the RF PA is the one that suffers the most from the requirements of CMOS technology. This is due to the fact that CMOS technology demands a low breakdown voltage, which limits the RF PA supply voltage [4].

In order to enhance performance, the amplifier was implemented as a conventional cascode, like the one presented in Figure 4. When compared to a one stage amplifier such as a common drain, the two stage cascode topology offers some advantages such as the reduction of losses caused by the Miller effect, higher power gain and higher bandwidth. In the next section, the efficiency of this cascode amplifier will be investigated.

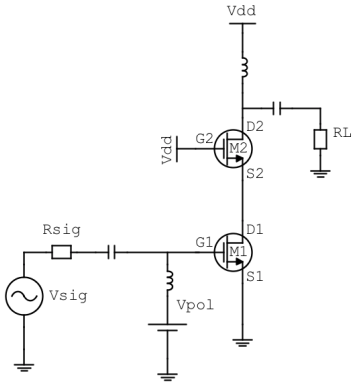

Figure 4 - Conventional cascode amplifier used as topology for the designed RF PA.

The need for high output power combined with the low supply voltage demanded by CMOS technology implies in a very low optimum load resistance for the RF PA. Notwithstanding, the output matching network must perform a high ratio impedance transformation from the optimum load to 50 ohm. Traditional

matching networks are designed with large capacitors and inductors, which induce large losses in the circuit due to their size. Furthermore, the lossy behavior of CMOS substrates significantly increases losses associated with passive elements.

In order to overcome this obstacle, [6] have proposed a combining power and matching impedance network known as Distributed Active Transformer (DAT), designed only with transformers. To deliver the desired power to the load, the whole power amplification system designed consisted of four identical RF PAs united by a DAT matching network. Figure 5 presents a simple block diagram of the design. DAT's major advantage is that the maximum output power delivered by one single RF PA is multiplied by a factor of 4. As a consequence, the optimum load resistance increases by the same factor, easing the impedance transformation process. Ideal transformer behavior was assumed for the DAT implementation having four primary windings and one secondary winding.

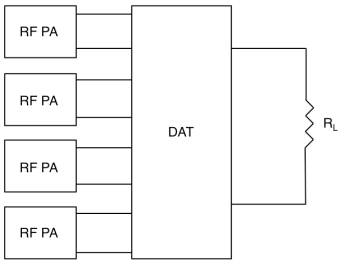

Figure 5 – Block diagram of the whole amplification network designed to operate as an RF PA.

6. COMPUTER SIMULATIONS

Both schematics shown in Figures 3 and 4 were designed in CMOS 130 nm technology with Cadence Virtuoso environment. Each single cascode RF PA has a central frequency of 2.5 GHz and an output power of 24 dBm at the 1 dB compression point.

Harmonic Balance (HB) simulations were performed in order to confirm the benefits of the ET network. The RF input signal was an amplitude-modulated signal (AM) given by:

$$s(t) = \left[A_2 + 2A_1 \cos(\omega_1 t)\right]\cos(\omega_2 t), \qquad (12)$$

where A_1 was set as 0.13 V, A_2 was set as 0.07 V, $\omega_1 = 20$ MHz and $\omega_2 = 2.5$ GHz.

To assess the average efficiency of the cascode amplifier, multi-tones HB simulations were performed. The first one kept the supply voltage constant and equal to 1.2 V. The average efficiency (defined by the ratio between the load power at the fundamental band and the power delivered by the DC sources) was 32.9%. In the second simulation, reproducing an ET network behavior on the circuit, the supply voltage source was replaced by a sinusoidal source with a waveform varying from 0.7 V to 1.2 V. The average efficiency, in this scenario, rose to 54.4%. Therefore, assuming an ideal EA, the ET network can improve the efficiency by 65.4%.

Assuming an ideal non-linear amplifier (i.e. average efficiency of 100%), a one-tone HB simulation was performed to obtain the average efficiency of the rail-to-rail class AB output stage of the EA. The envelope of (11) was applied as the EA input and the output power level was adjusted so that the voltage swing was as close as possible to the desired RF PA supply. When the EA output voltage swung from 0.51 V to 1.02 V the average efficiency of the class AB was 31.0% and the overall efficiency of the EA was 88.7%. For this work, it is important to notice that the largest amount of power is DC and is being amplified by an ideal switching amplifier.

The product of the RF PA and the EA efficiency gives the ET overall efficiency. For this study, it corresponds to 48.3%, which means that the ET network can improve the efficiency by 46.8%.

7. CONCLUSION

This work confirmed the benefits of the Envelope Tracking amplification network by designing its two main blocks and analyzing their behaviors alone and integrated in such a system. Each single RF PA achieved an output power of 24 dBm at 1 dB compression point.

For the RF PA, in an ideal situation, it was possible to raise the efficiency response from 32.9% (with constant supply voltage) to 54.4% (with controlled supply voltage). The overall efficiency of the designed EA was 88.7%. When integrating both circuits, the overall efficiency achieved was 48.3%.

8. ACKNOWLEDGMENTS

The authors would like to acknowledge the financial support provided by *Conselho Nacional de Desenvolvimento Científico e Tecnológico* (CNPq) under the Program of *Iniciação em Desenvolvimento Tecnológico e Inovação,* UFPR 2013-2014.

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