Design and Linearity Analysis of a M–2M DAC for Very Low Supply Voltage

ABSTRACT

This work presents the design of a 6 bits M-2M ladder Digital-to-Analog Converter (DAC) proper for operation under supply voltages of 200 mV or lower. Since the MOS transistors are operating in the subthreshold region under such low supply, the mismatch analysis was done using an all-region continuous MOSFET model. The performance of the circuit is evaluated through simulations and the trade-offs between linearity, supply voltage and different threshold devices are investigated in the paper. It is proposed that a 6 bits M-2M DAC operating under 200 mV is feasible using standard transistors and Low-V_T transistors from a commercial 130 nm process.

Categories and Subject Descriptors

B.4 [**Very Large Scale Integration Design**]: Analog and Mixed-Signal Circuits—*Data conversion*

Keywords

DAC, Low-Voltage, UICM Model, Inversion Level

1. INTRODUCTION

The continuing scaling of CMOS technologies is the main driving factor behind low voltage operation, rapidly achieving sub-1 V supplies for process nodes below 130 nm. Current battery-operated systems require ultra-low current operation, that ranges from a few nanoamperes to a few microamperes, depending on the function being executed. Also future self-powered and self-sustaining electronic systems will require ultra-low voltage (ULV) operation, since the physical or chemical environmental strategies that can be used for energy harvesting generates from 10's to a few 100's of millivolts. And focusing on this perspective, data-converters that could operate under ULV condition will also be a fundamental class of mixed-signal CMOS circuits.

A survey on the evolution of Analog to Digital Converters (ADC) performance was made by Jonsson [1] in 2010.

From this research we can highlight the decrease of the supply voltage through the years showing that designers are always trying to achieve the lowest supply voltages on each technology node. Most recent results are showing that it is possible to build converters with 6-bits of resolution and 200mV of supply [2]. Taking this into account and keeping in mind that the Digital to Analog Converter (DAC) is the key block of an ADC, this work suggests the use of a M–2M DAC as a convenient choice for operation under low voltage conditions.

The M–2M DAC is a MOS-only version of the R–2R ladder network, and it was proposed by Bult and Geelen in 1992 [3], using the current division property of the MOS transistors. They noted that two series-connected MOS transistors, with the same size and gate voltage, equally divide the current applied on their common terminal, regardless the voltage applied on the other terminals or the operation region. Since then, this topology was already published in other DAC applications [4].

In this work we continue the study of the CMOS M–2M ladder operating with very low supply voltages [5], including its linearity analysis and the use of different threshold devices.

The paper is organized as follows. In section II the all-region MOSFET model is reviewed. In section III the basic structure of the M–2M DAC is presented and analysed for any operation region, and the design methodology is presented. In section IV the simulation results for the DACs are presented, while section V presents our main conclusions.

2. MOSFET MISMATCH MODEL

The M–2M DAC network operates doing a binary current scaling where the current division errors are related to the matching among the MOS transistors that compose the ladder, defining the entire DAC linearity. Since the linearity of the DAC is related to its effective resolution, a mismatch accurate model of the MOSFET is necessary.

The Unified Current Control Model (UICM) [6], is a physics-based all-region MOSFET model that uses the "inversion level" parameter, and provides the basis of our analytical formulation.

This model represents the drain current of a transistor as the sum of two opposite current components, a forward (I_F) and a reverse (I_R) one

$$I_D = I_F - I_R = I_{SQ}\frac{W}{L}(i_f - i_r) \qquad (1)$$

where $I_{SQ} = \frac{1}{2}\mu C'_{ox}n\phi_t^2$ is the sheet normalization current,

(W/L) is the aspect ratio, n is the slope factor, μ is low field mobility, C'_{ox} is the oxide capacitance per unit of area and ϕ_t is the thermal voltage. Parameters i_f and i_r are the normalized forward and reverse currents, or "inversion levels", at source and drain, respectively.

The forward and the reverse inversion levels are also related to the terminal voltages as follows

$$V_G - V_T - nV_{S(D)} =$$
$$= n\phi_t \left[ln\left(\sqrt{1+i_{f(r)}} - 1\right) + \sqrt{1+i_{f(r)}} - 2 \right] \quad (2)$$

where V_G, V_S and V_D are the gate, source and drain voltages refered to the bulk potential, respectively, and V_T is the threshold voltage.

A MOSFET mismatch model based on the UICM model was proposed in [7], being more appropriate to the DAC non-linearity analysis than the traditional Pelgrom's mismatch model [8], which does not consider the subthreshold non-linear nature of MOSFETs in a proper way. The following equation presents the dependency of the current mismatch on the transistor area, on the inversion levels and on the technology parameters

$$\frac{\sigma_{I_D}^2}{I_D^2} = \frac{1}{WL} \left[\frac{N_{oi}}{N^{*2}} \frac{1}{i_f - i_r} \ln\left(\frac{1+i_f}{1+i_r} \right) + B_{I_{SQ}}^2 \right] \quad (3)$$

where $N^* = nC'_{ox}\phi_t/q$ is the carrier density at pinch-off condition, N_{oi} is the main mismatch model parameter, related to the number of impurity atoms inside the depletion volume under the channel area, and $B_{I_{SQ}}$ is a less significant model parameter that accounts for variations in the specific normalization current I_{SQ}.

3. CIRCUIT DESCRIPTION AND DESIGN METHODOLOGY

The ladder network shown in Fig. 1 is formed by a sequence of M–2M cells, one per bit, and finalized by a 2M termination. In general this ladder is formed by cells with transistors having the same geometry, simplifying the layout. Each cell divides its input current by half, performing the DAC weighting through successive binary divisions of the reference current I_{Ref} generated by V_{Ref}. The two drain–connected transistors M_2 and M_3 deviates the binary fraction of the current to I_{out} or $\overline{I}_{out}$ node, depending on the S_i switch state, since these nodes are tied to ground through a very low impedance connection, resulting for any binary combination that $I_{Ref} = I_{out} + \overline{I}_{out}$.

The switches are implemented with transmission gates driven by a digital register that stores the input binary data. In this work we do not explore the register design since our main focus is the ladder current division linearity analysis. Digital circuits like logical gates and registers operating with very low supply voltages have already been studied in recent works [9].

Finally, the current summing that results in the I_{out} node represents a binary proportion of I_{Ref}, controlled by the input digital data. A detailed analysis of this network can be found in [10]. The four identical MOSFETs on each cell result in a very regular and compact layout that improves matching.

The analysis of resulting inversion levels of the transistor terminals that are needed in this design were thoroughly explained in [5]. This design method was implemented in MatLab to create a tool that can estimate the statistical
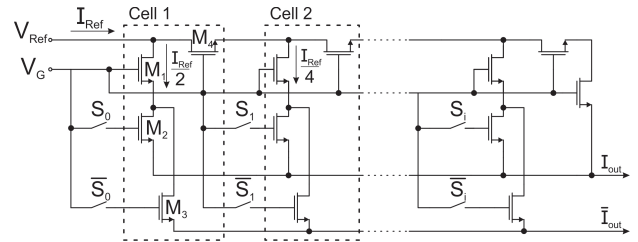

Figure 1: M–2M CMOS Ladder Network.

error of an M–2M DAC, in terms of the standard-deviation of the output current σ_{Err}, when related to the ideal linear behavior. In Fig. 2 this error (expressed as a fraction of the LSB related to the intended resolution) is shown as a function of the transistor area, for two supplies (100mV and 200 mV). The estimated error is performed for a given bias (V_G and V_{Ref}), resolution (the depth of the ladder), and individual transistors size (W and L).

4. SIMULATION RESULTS

The method was applied to a M–2M DAC with 6 bits of resolution, implemented in the IBM 130 nm process using standard NMOS transistors ($V_T = 200mV$ for long channel FETs) and Low–V_T NMOS transistors ($V_T = 100mV$ for long channel FETs). Equal values for V_G and V_{Ref} were chosen to simplify the analysis ($200mV$ and $100mV$), corresponding to moderate and weak inversion regions. The design uses $L = 10\mu m$ as a way to avoid short-channel effects [10].

The mismatch parameter $B_{I_{SQ}}$ on equation (3) was obtained from the process PDK ($3\% - \mu m$ for the standard transistors and $6\% - \mu m$ for the Low–V_T transistors). N_{oi} can be estimated from the A_{V_T} mismatch parameter of the Pelgrom's model [11], using $\sqrt{N_{oi}} = \frac{C'_{ox}A_{V_T}}{q}$, resulting $N_{oi} = 7 \cdot 10^{13}cm^{-2}$ for the standard transistors and $N_{oi} = 6.5 \cdot 10^{13}cm^{-2}$ for the Low–V_T transistors.

The Fig. 2 presents the estimated DAC error using the methodology described in the last section, for the two biasing voltages and related to the individual transistor area, being useful for design-space exploration. In this work we kept the same inversion levels for all transistors in the two different converters, which means that for the Low–V_T devices the same inversion level is achieved with lower supply, so, $V_{Ref} = V_G = 107mV$ for $i_f = 4.5$. To achieve an inversion level of 0.24 on the Low-V_T transistor we have to consider using supplies around 10 mV which starts to introduce some non-linearities that are out of the scope of this work.

As a way to validate the presented linearity analysis methodology, the M–2M DAC was designed and simulated using the Cadence-Virtuoso tool. Monte-Carlo (MC) simulation with 500 runs was performed, and the error standard deviation ($\sigma_{err}(LSB)$) was calculated and normalized to the nominal LSB.

Based on the area trend shown in Fig. 2, we chose the aspect ratio for the 6-bit converter equal to $\frac{W}{L} = \frac{25\mu m}{10\mu m}$ for each transistor. The final circuit layout using the standard–V_T is shown on Fig. 3, resulting a silicon area of $0.024mm^2$, including the data register and the dummy structures for matching improvement. The layout using the Low–V_T tran-
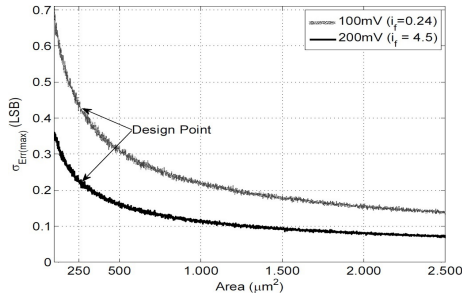
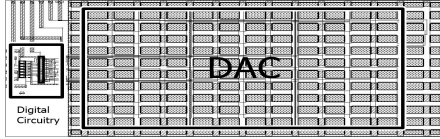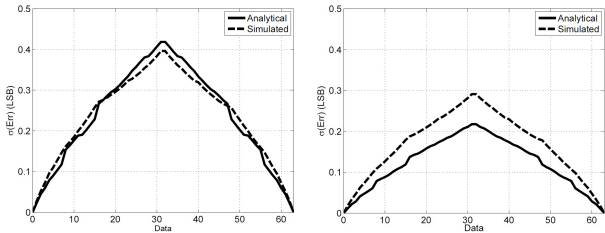Figure 2: Standard deviation of the DAC error as a function of individual transistor area and biasing voltage.
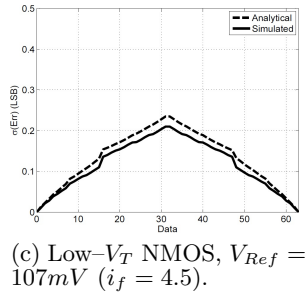

Figure 3: DAC layout with standard NMOS transistors.

(a) Std. NMOS, $V_{Ref} = 100mV$ ($i_f = 0.24$).

(b) Std. NMOS, $V_{Ref} = 200mV$ ($i_f = 4.5$).

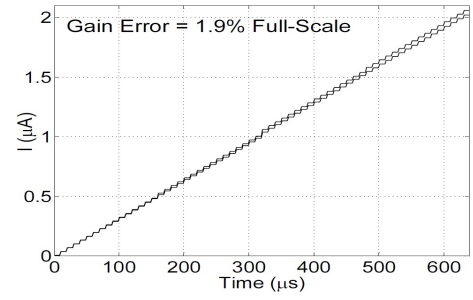(c) Low–V_T NMOS, $V_{Ref} = 107mV$ ($i_f = 4.5$).

Figure 4: Comparison between analytical and post-layout simulated results of a 6-bit converter.
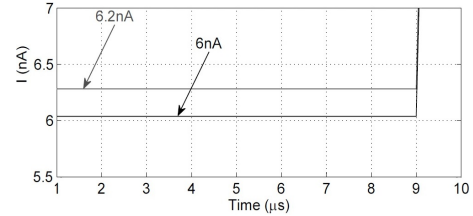
sistors is very similar.

Analytical and simulated results can be seen in Fig. 4a and Fig. 4b using biasing voltage V_{Ref} equal to $100mV$ (inversion level $i_f = 0.24$, corresponding to weak inversion) and $200mV$ (inversion level $i_f = 4.5$, corresponding to moderate inversion).

For the Low–V_T transistor (Fig. 4c) we have almost the same result of Fig. 4b, which is expected, since we kept both in the same inversion level and the transistor mismatch parameters are similar.

Since analytical and simulated results are similar, we suppose that our methodology can be used for trade-off estimation and design-space exploration of M–2M DACs operating under very low supply voltage.

(a) Gain error.

(b) Offset error.
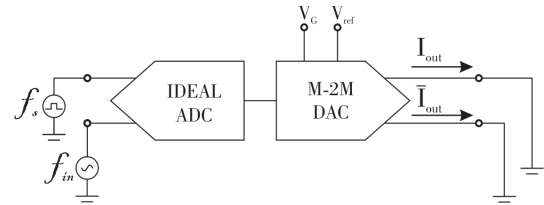
Figure 5: DAC linear gain and offset errors.

Figure 6: Testbench topolgy for the spectral analysis.

4.1 Gain and Offset Considerations

Considering that the DAC works with extremely low gate voltages, the difference between the "on" and "off" states of the switching transistors (M_2 and M_3 for example) is small, but it does not cause significant linearity reduction, impacting only as offset and gain errors, that are linear characteristics and can be easily calibrated. To illustrate this behavior we depicted the two worst cases of the Monte Carlo simulation in Fig. 5, where one can see the gain error (Fig. 5a) and the offset ("zero") error (Fig. 5b), that is a zoomed part of the gain error figure. This figure was obtained exciting the DAC digital input with a progressive binary code that changes from "0" to "63" in steps with 10 microseconds of time duration.

4.2 Spectral Analysis

In order to evaluate the converter sampling speed we used the testbench shown in Fig. 6, that consists on a 6 bits verilog ideal ADC with variable clock that converts a sinusoidal analog input signal to its digital counterpart, to be used as the DAC input. The signal frequency and the ADC clock varies following the relationship $f_i = \frac{J}{M} f_s$, being f_i the input frequency, f_s the sampling frequency (clock), J the number of cycles and M the record length. We also ensured that J and M have no common factors [12].

On Fig. 7 the ADC input and DAC output waves are presented for post-layout simulation of both DACs, with standard and Low–V_T transistors. We can see that the converter
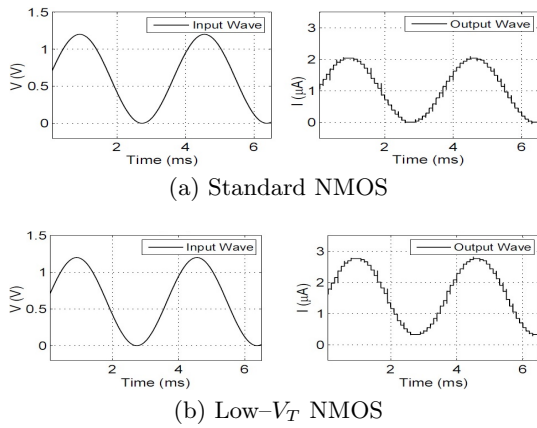
(a) Standard NMOS

(b) Low–V_T NMOS

Figure 7: ADC input and DAC output waves.
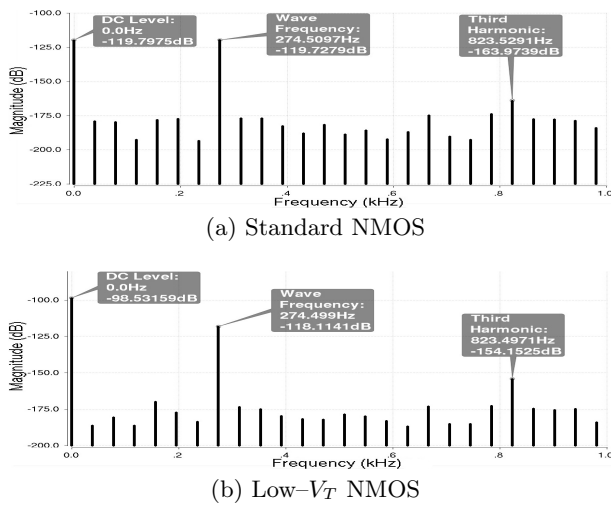

(a) Standard NMOS

(b) Low–V_T NMOS

Figure 8: Discrete Fourier Transform of the DAC output signal.

clearly reconstructs the input signal after some switching glitches are removed by a low pass filter.

Still regarding the input wave, for a clock frequency of $10kHz$ with 7 cycles and 255 samples we obtained $f_i = 274.5Hz$. Using the Spectrum Measurement tool on Virtuoso we can plot the discrete fourier transform (DFT) of the output signal (Fig. 8), that shows a difference of 44 dB between the the signal frequency and the Third Harmonic Distortion for the standard device, indicating an Effective Number of Bits (ENOB) of 7 bits. For the Low–V_T devices DAC the difference is 36dB indicating an ENOB of 5.7 bits.

The aforementioned results corroborate that the M–2M DAC is a promising topology for very low voltage applications, being possible to implement a 6-bit DAC with standard transistors. The converter behavior is similar for the Low–V_T DAC, although it presented a higher distortion that caused the ENOB reduction showed on Fig. 8b.

5. CONCLUSION

In this paper we presented the design analysis of the MOSFET M–2M DAC operating under very low supply voltages. A design methodology that can be used for design-space ex-

ploration and trade-off estimation was presented and a 6-bit DAC was designed in a 130 nm process, proper for operation under $200mV$, consuming a silicon area of $0.024mm^2$. Monte-Carlo simulations supported our analytical approach and a testbench was used to predict the spectral behavior of the DAC, resulting on ENOBs of 7 bits for the standard transistor and 5.7 bits for the Low–V_T transistor.

6. REFERENCES

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