FPGA-Based Implementation of a Biomedical Signal Processing Unit for Bioimpedance Measurement Application

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ABSTRACT
Bioimpedance is an electrical property of biological tissues and its measurement has been used for a wide range of applications such as disease diagnosis or to estimate body composition. This paper describes the design of a four-electrode single frequency bioimpedance digital meter based on a direct digital measurement technique which was implemented using Xilinx System Generator (XSG) for Matlab. Rapid prototyping tools such as XSG simplify the design of digital systems by enabling the designer to shorten design time and to verify the projected model functionality before its final implementation on hardware in a very efficient way through co-simulations of hardware and software. The architecture presented in this paper for the phase and magnitude measurement was implemented in VHSIC Hardware Description Language (VHDL) code and imported to the Matlab/Simulink environment as black boxes targeting the Digilent GenesysTM Virtex 5 FPGA. The architecture was simulated in Simulink and later validated using a hardware/software (HW/SW) co-simulation approach. According to obtained results, the direct digital measurement (DDM) technique has shown low FPGA resource usage, low power consumption and low error margins.

Keywords
Bioimpedance; FPGA; co-simulation; Xilinx System Generator; Direct Digital Measurement.

1. INTRODUCTION
Bioelectrical impedance is the resistance that biological tissues offer to an electric current flow. Therefore, it is related to the electrical properties of a tissue [1]. The study in this field has significantly increased lately and a lot of researches have been conducted since the first description of the tissues electrical characteristics in 1871 [1,2] and several methods for bioimpedance measurements are now available [1,3].

Among the main methods available for measuring bioelectrical impedance, the most common is the four-electrode technique, where the phase difference, used in measuring the bioelectrical impedance is calculated by the injection of a reference current onto the tissue through a pair of electrodes and the measurement of a respective resulting voltage on the tissue by another pair of electrodes [4]. Since bioimpedance is a complex division of the measured voltage by the reference current injected on the tissue it is necessary to measure the phase difference between both signals as well as the magnitude ratio.

Signal processing for bioimpedance calculations and also to estimate the correlations between a characteristic of the human body or any other biological tissue can be achieved by digital or analog electronic circuits. Bioimpedance Analysis (BIA) devices have often been built based on Application-Specific Integrated Circuits (ASICs) or reconfigurable hardware, which can handle high frequencies and parallel processing [5,6]. Digital Signal Processing (DSP) integrated circuits (IC) are also used for bioimpedance measurement. Nevertheless, DSP ICs have limited frequency ranges and restricted number of storage points on top of high power consumption [7]. Lately, FPGAs have been often used in digital signal processing, as a result of their versatility, their high density of transistors, the ability to meet computational, power consumption and memory requirements along with the great advantage of reconfigurability, which leads to rapid hardware prototyping and efficient testability [7-9].

A phase difference measurement system based on a direct phase measurement technique is presented in [10]. In this technique, a pulse counter is used for phase measurement between the signals. This pulse counter counts for a period of time proportional to the phase difference. Moreover, a recent work [3] proposes a Synchronous Phase Detection System (SPDS) implemented using XSG as a solution for measuring phase difference, which is used to estimate bioimpedance in a four-electrode 50 kHz single frequency BIA system.

This paper describes the design of an FPGA-based Bioimpedance Measuring System (BMS) composed by a customized version of a Direct Digital Measurement (DDM) approach presented in [10] and a Peak Magnitude Detector (PMD) as a solution for 50 kHz single frequency four-electrode BIA systems and its validation using HW/SW co-simulation. Additionally, a brief comparison with the results obtained in [3] is also presented.

2. SINGLE FREQUENCY BIA
As stated before, bioimpedance can be calculated through the complex division of the voltage measured over a certain tissue under test and a reference current injected through electrodes on the tissue. BIA became one of the main methods for obtaining biological data from biological tissues by the use of electronic systems. It has been broadly used in nutritional and clinical

diagnosis, since the medical validation of the correlations between the human body physiology and the impedance measurement of its related biological tissues that happened in the 90s [5]. Furthermore, as a common mechanism of signal transduction for analysis of body composition and diagnostic assessment, it is recognized as noninvasive, reproducible, reliable, for having low cost and for being of easy analysis [1,5,11,12]. Although the amount of clinical applications has become commercially available very slowly through the years, physiological measurements derived from the bioimpedance analysis are widely used in a large number of medical applications, as a method to diagnose cancer and several other diseases as well as for non-medical applications, such as to estimate the quality of wood or even beverages such as milk and beer [1].

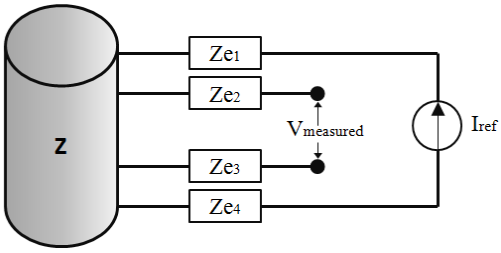

Figure 1. Tetrapolar measuring system basic configuration (adapted from [3])

One of the most primitives and the most common method for bioimpedance analysis is referred to as single-frequency bioimpedance analysis (SF-BIA), which uses a 50 kHz current as the reference signal in a tetrapolar configuration [11]. In this work a SF-BIA system is proposed. Figure 1 shows the basic configuration of a tetrapolar measuring system, also known as four-electrode method. In this method, the 50 kHz reference current is injected onto the tissue and a voltage drop is measured over the tissue. This method has been used for decades and presents the major advantage of cancelling the parasitic currents generated at the interface between electrodes and tissues [3,4]. Additionally to the measuring system, amplifiers are used to scale the measured signals and a low pass filter should be used to reduce high frequency noise. The final stage of a BIA system is called Bioimpedance Computing Stage (BCS) and it is responsible for calculating the bioimpedance based on the data obtained or even deliver a biological parameter as an output [5].

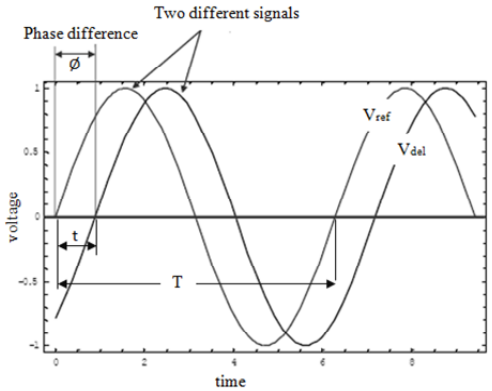

Figure 2. Phase relationship between two signals (adapted from [13])

3. DDM PHASE SHIFT METER

The phase difference between two signals can be obtained by measuring time or direct phase measurement. However, measuring phase shift by time measurement requires complex calculations to determine what the phase is [10]. Figure 2 shows the phase difference between two signals. V_{ref} represents the reference signal, while V_{del} represents the delayed signal. In a bioimpedance measuring system, V_{ref} would probably be an injected current over the tissue and V_{del} would be the measured voltage drop through the same tissue. The phase relationship between the two signals (Ø) can be expressed in terms of the period T of the reference signal, and delay time t of the delayed signal, as shown in (1).

$$\emptyset = 360 \cdot \left(\frac{t}{T}\right) \quad (1)$$

Both the measurements of the delay time and period are made by a counter triggered by a clock that has a previously defined frequency f_c. Thus, for a given time interval t, N pulses are counted and the period will be $1/f_c$. This relationship is presented in (2). Replacing (2) in (1), we obtain the equation (3) that relates the phase difference to the number of pulses counted and the frequencies used, where f is the frequency of the reference signal.

$$t = N \cdot \left(\frac{1}{fc}\right) \quad (2)$$

$$\emptyset = \left(\frac{360 \cdot f}{fc}\right) \cdot N \quad (3)$$

Equation (3) shows that through this method, a phase angle can be measured directly if the rate between f_c and f is set to be a value in the form of 3.6×10^n. In this case, the number of measured pulses and the phase angle are related according to (4). If we consider a delay of one degree, we can use equation (4) to calculate Ø. Additionally, (5) is used to determine the clock frequency that related to the reference signal frequency will result in the desired angular resolution.

$$\emptyset = \left(\frac{N}{10^{n-2}}\right) \quad (4)$$

$$fc = 3.6 \times 10^n \cdot f \quad (5)$$

An adapted version of the digital phase meter presented in [10] is shown in Figure 3. When the measured signal represented by $V_{del}(t)$ switches from negative to positive, CD, which is a comparator, outputs a pulse that triggers a start pulse. The start pulse sets the flip-flop RS to a high logic value and enables the AND gate to work as a buffer for the pulse of frequency f_c, which then works as a clock to the counter. When $V_{ref}(t)$ changes from negative to positive, it triggers a stop pulse that stops the counting. The counter must be reset before a new cycle.

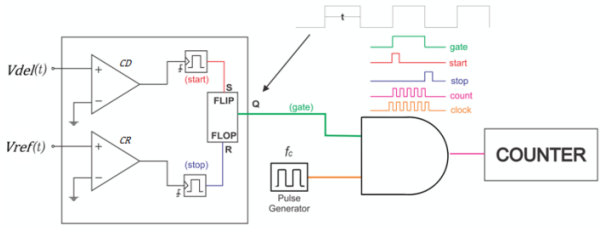

Figure 3. Phase shift meter by pulse counting (adapted from [10])

Since a magnitude meter is also needed for the bioimpedance measuring system, a PMD is presented in figure 4. It basically works based on the concept of zero crossing. When a sampling clock rising edge occurs, if a zero crossing is detected, then the maximum value is set to the lowest possible value, and the minimum value is set to the maximum possible value. Otherwise, the input signal sample is stored in the new value buffer and a

subsystem is activated according to the signal value. If subsystem 1 is activated, if the stored new value is greater than the actual maximum value, the subsystem 1 updates the maximum value with the new stored value. On the other hand, if subsystem 2 is activated and the new stored value is lower than the current minimum value, the subsystem 2 updates the current minimum value, otherwise, it loads the actual stored minimum value into the output buffer. However, if subsystem 3 is activated, a zero value is loaded into the output buffer. Finally, a zero crossing detection resets the minimum and maximum values preventing the magnitude detector to stand on hold of an old value. Additionally, a positive semi-cycle outputs the highest value found just when the input signal starts to decay for a lower value. Likewise, the negative semi-cycle outputs the lowest value just when the input signal starts to increase for a greater value. This prevents no peak values to be loaded into the output buffer.

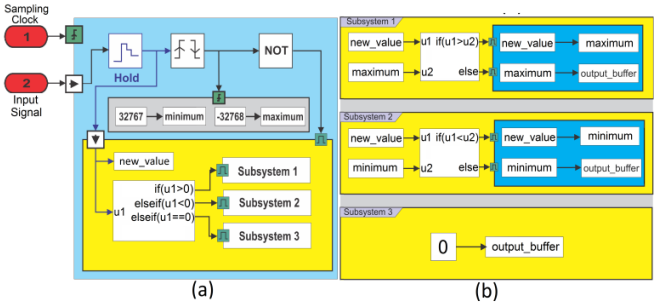

Figure 4. Magnitude measuring system diagram, composed by a (a) peak magnitude detector main block and (b) its subsystems

4. DESIGN METHODOLOGY

4.1 Xilinx System Generator (XSG)

For systems that require complex computations, generally designers prefer to use hardware instead of software processing and FPGAs have often been chosen as an attractive solution for embedded systems because of its high performance [9]. However, traditional implementation of FPGA-based embedded systems presents a few disadvantages. In traditional VHDL designs, there is a need for an extra code to be written in order to test it. Another drawback is that the simulation cannot interact with other models and some faults can only be noticed after final implementation in hardware [14].

Xilinx System Generator for DSP is a toolbox for Simulink that offers to designers a wide range of blocks which can all be integrated with Matlab/Simulink models. While using XSG, the designer can either use high-level blocks, which are very helpful for complex systems design [9], or import VHDL codes to the Simulink environment as black boxes. XSG also performs synthesis, place and routing automatically, translating all the Xilinx blocks into an FPGA bitstream file [9,15]. One of the main advantages of XSG is to enable designers to simulate the design integrated with Simulink models, which can be very useful for HW/SW co-simulation and for rapid prototyping and testing when there are time-to-market constraints. The system validated and presented in this paper was designed targeting a Digilent Genesys Virtex-5 FPGA development board based on a Xilinx Virtex-5 LX50T, which is the board available in our research lab.

4.2 Simulation

The DDM system proposed as a solution for a BMS was fully implemented in VHDL and imported to the XSG/Simulink environment and was then simulated. The output of the PMD and also from the DDM phase-difference meter was designed to be a 16-bit signed 2's comp integer number. The PMD sampling frequency chosen was 2 MHz. With equations (4) and (5) we calculated the counter frequency f_c, based on an accuracy of 0.1º and a reference signal with 50 kHz, which resulted in an f_c of 180 MHz. In order to not violate the Nyquist criterion, the FPGA clock frequency was set to be 360 MHz.

The 50 kHz reference signal generator and the ADC output were built with discrete look-up tables, consisting of 100 points designed as 8-bit signed 2's comp integers. This design strategy leads to an accuracy of 3.6 ° and an ADC sampling frequency of 5MHz. The reference sine and cosine signals have unitary amplitude. The reference current has a magnitude of 1 mA at a zero degree phase angle.

4.3 HW/SW Co-Simulation in XSG

As mentioned before, the system designed was synthesized and downloaded and run onto an FPGA through a HW/SW co-simulation, which was performed using XSG to validate the system proposed. A co-simulation library was created based on the model created for the simulation described in the previous step, targeting a Xilinx Virtex-5 LX50T FPGA. Figure 5 shows the implemented XSG model. After all, the timing and power analysis of the XSG tool was also run, to verify power consumption and clock constraints.

5. RESULTS AND DISCUSSIONS

The system designed, presented a very similar behavior in the Simulink simulation and in the HW/SW XSG co-simulation. In figure 6, the results from the hardware co-simulation of the phase difference meter are presented. As we can see, the system proposed has a very precise linearity in almost all the measured ranges with resolution of 0.1º.

Table 1 shows some of the obtained values of bioimpedance along with the expected measurements. Besides that, table 1 also

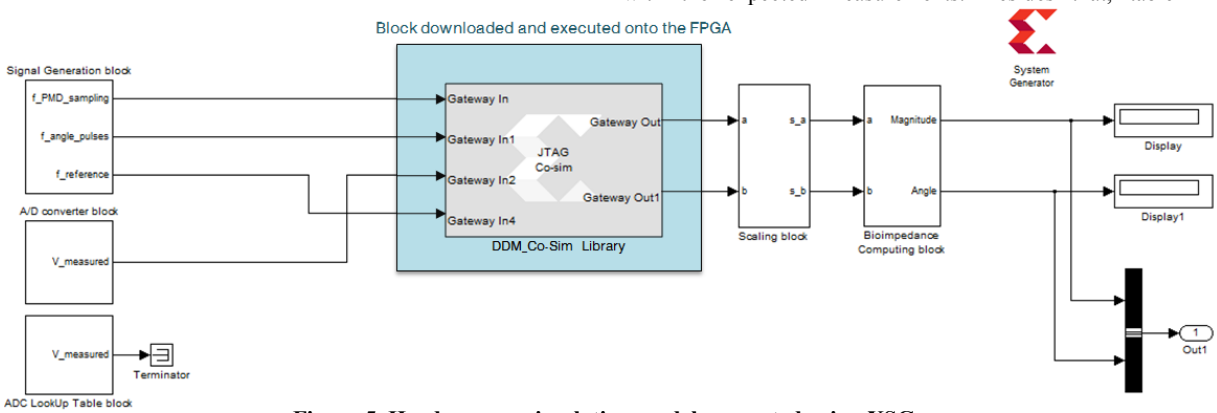

Figure 5. Hardware co-simulation model generated using XSG

introduces the calculated errors between the obtained and the expected bioimpedance values. For comparison purposes, the gray section on table 1 shows the results presented in [3], which proposes a similar BIA system based in a SPDS, as mentioned before. As we can observe, the DDM technique proposed has presented lower error margins.

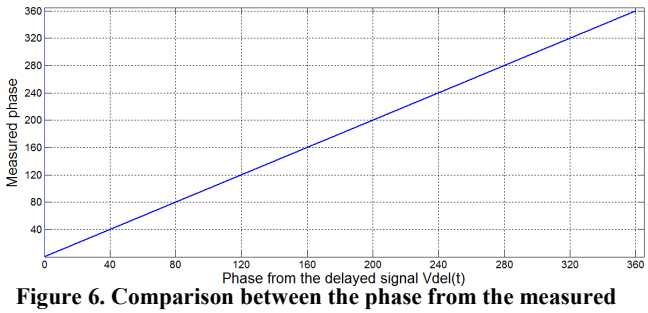

Figure 6. Comparison between the phase from the measured and delayed signals

Table 1. Bioimpedance Obtained Results

Phase Ø	Expected Bioimpedance (Ω)		Obtained Bioimpedance (Ω)		Error (%)	
	Real	*Imag.*	*Real*	*Imag.*	*Real*	*Imag.*
0°	0°	1	0	0.9998	0	0.02
72º	72º	0.3090	0.9511	0.3089	0.951	0.03
144º	144º	-0.8090	0.5878	-0.8088	0.588	0.03
288º	288º	0.3090	-0.9511	0.3089	-0.951	0.03
0°	0°	1	0	0.9992	0	0.08
72º	72º	0.3081	0.972	0.2996	0.9622	2.76
144º	144º	-0.8161	0.5774	-0.8039	0.5664	1.49
288º	288º	-0.294	0.9674	-0.2894	0.9384	1.56

Table 2 compares the resource usage with the total hardware available in the FPGA. As it is shown, the model proposed uses a very low amount of the resources available.

According to the XSG Timing and Power analysis tool, the maximum clock that can be achieved by the Genesys development board is 599.520 MHz and for an environment temperature of 30 ºC, the power consumption of the overall system would be only 460 mW (92mA@5.0V). This power consumption is less than 3% of the total power available in Genesys power supply and since almost 98% of this power is due device static power, we'll notice that the system designed presents very low power consumption. As we can observe, the FPGA used for this design meets the minimum frequency requirements and has an acceptable overall power consumption to perform the digital signal processing and calculations.

Table 2. Model Resource Usage

	Resources Available	Resources Usage	Amount (%)
Slices	7,200	73	1.01
FFs	28,800	121	0.42
LUTs	28,800	158	0.55
IOBs	480	51	10.6
MUlts/DSP48s	48	0	0.00

6. CONCLUSIONS

The design, simulation and validation of an FPGA-based single-frequency tetrapolar bioimpedance digital meter using a Direct Digital Measurement (DDM) technique and Xilinx System Generator (XSG) were presented in this paper. The obtained results have shown that despite the high FPGA clock frequency required, the model proposed presents very low resource usage (less than 10% of the total resources available), very low power consumption and low error margins.

7. REFERENCES

[1] Grimnes, S. and Martinsen, O.G. 2008. *Bioimpedance & Bioelectricity Basics*, 2nd ed., Oxford, UK:Elsevier.

[2] Kyle , U.G., Bosaeus, I., De Lorenzo, A.D., Deurenberg, P., Elia, M., Gómez, J.M., Heitmann, B.L., Kent-Smith, L., Melchior, J., Pirlich, M., Scharfetter , H., Schols, A.M.W.J. and Pichard, C. 2004. Bioelectrical impedance analysis—part I: review of principles and methods. *Clinical Nutrition*, vol.23, pp. 1226-1243, DOI= 10.1016/j.clnu.2004.06.004

[3] Martinez-Nolasco, C., Diaz-Carmona, J., Prado-Olivarez, J., Ramirez-Agundis, A. and Padilla-Medina, A. 2012. FPGA Synchronous Phase Detection System for bioimpedance computing applications. in *Circuits and Systems (MWSCAS)*, 2012 IEEE 55th International Midwest Symposium on, pp.362,365, 5-8. DOI= 10.1109/MWSCAS.2012.6292032

[4] Ivorra, A. 2003. *Bioimpedance Monitoring for physicians: an overview*, Centre Nacional de Microelectrònica.

[5] Oliveira, A.C., Pereira, R.C.M., Dias, J.S., Leite, B.R.B.A. and Mariano, A.A. 2015. A comparison between direct digital measurement technique and digital quadrature demodulation for complex bioimpedance measurement implementation in FPGA. in *XXI Iberchip Workshop*, Montevidéu, IWS 2015

[6] Odry, P., Henezi, F., Burkus, E., Halasz, A., Kecskes, I., Marki, R., Kuljic, B., Szakall, T., Máthé, K. 2011. Application of the FPGA technology in the analysis of the biomedical signals. *Intelligent Systems and Informatics (SISY)*, IEEE 9th International Symposium on , vol., no., pp.407,412, 8-10 Sept. 2011, DOI=: 10.1109/SISY.2011.6034362

[7] Veiga, E.A. and Bertemes-Filho, P. 2012. Bioelectrical impedance analysis of bovine milk fat. *Journal of Physics: Conference Series*, vol. 407. IOP Publishing, DOI= 10.1088/1742-6596/407/1/012009

[8] Woods, R., McAllister, J., Lightbody, G., Yi, Y. 2008. *FPGA-based Implementation of Signal Processing Systems*, West Sussex, UK: Wiley

[9] Moreo, A.T., Lorente, P.N., Valles, F.S., Muro, J.S., Andrés, C.F. 2005. Experiences on developing computer vision hardware algorithms using Xilinx system generator. *Microprocessors and Microsystems*, vol. 29, issues 8–9, Nov. 2005, pp. 411-419, DOI= 10.1016/j.micpro.2004.11.002

[10] Rathore, T. S. 2009. *Digital Measurement Techniques*, 2nd ed., India: Alpha Science.

[11] Khalil, S., Mohktar, M. and Ibrahim, F. 2014. The Theory and Fundamentals of Bioimpedance Analysis in Clinical Status Monitoring and Diagnosis of Diseases. *Sensors*, vol. 14, no. 6, pp. 10895–10928. DOI= 10.3390/s140610895

[12] Colín-Ramírez, E., Castillo-Martínez, L., Orea-Tejeda, A., Vázquez-Durán, M., Rodríguez, A.E., Keirns-Davis, C. 2012. Bioelectrical impedance phase angle as a prognostic marker in chronic heart failure. *Nutrition,* vol. 28, no. 9, pp. 901-905 DOI= 10.1016/j.nut.2011.11.033.

[13] Wyant, J.C. *Direct Phase Measurement Interferometry*. College of Optical Sciences, Retrieved from the University of Arizona: http://fp.optics.arizona.edu/jcwyant/Optics513/ChapterNotes/Chapter05/05-1-Direct_Phase_Measurement_Interferometry.pptx.pdf

[14] Thangavelu, A., Varghese, M.V., Vaidyan, M.V. 2012. Novel FPGA based controller design platform for DC-DC buck converter using HDL Co-simulator and Xilinx System Generator. in *IEEE Symposium on Industrial Electronics and Applications (ISIEA)* , vol., no., pp.270,274, 23-26 Sept. 2012, DOI= 10.1109/ISIEA.2012.6496642

[15] Raut, N.P., Gokhale, A.V. FPGA Implementation for Image Processing Algorithms Using Xilinx System Generator. *IOSR Journal of VLSI and Signal Processing*. India, IOSR-JVSP, DOI= 10.9790/4200-0242636