Redesigning state-of-the-art QCA Adders in NML Technology

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***Abstract*—Nanomagnetic Logic (NML) is a very promising technology to substitute CMOS, since the later will soon reach its physical limitations. NML offers great advantages, such as low energy consumption, computation in room temperature and very small size. In this work we propose to implement in a NML simulator 3 state-of-the-art adder topologies that have been previously implemented in Quantum Cellular Automaton (QCA) technology. Moreover, we show the main differences and challenges of redesigning QCA circuits in NML technology.**

***Index Terms*—NML, QCA, adders, Nanomagnetic Logic.**

I. INTRODUCTION

It is notorious how small and fast the transistor have become with the advances of technology along the years. CMOS technology reached optimum results in the development of integrated circuits due the great advances of transistor, but their scale size cannot keep decreasing indefinitely [1]. Also the energy demanded to simply maintain the data in the circuits is almost reaching the same level as the amount needed to perform computation. These limitation are one of the main problems which the semiconductor industry is facing to continue the expectations of the Moore's Law [5].

Among many alternative technologies to CMOS, QCA and NML are two good promising nanotechnologies to take place over CMOS. QCA is a nanoscaled square cell which contains four quantum-dots and two electrons [6]. Each dot is located in the corner of the cell and can hold one electron at a time, making possible two configurations due the Coulomb repulsion, as shown in Figure 1. Using each of these configuration as a binary encoding, computation is possible to be realized. Although QCA solves some of the limitations of CMOS, such as miniaturization and high switching speed, the QCA devices bring its own, such as the impossibility to operate in room temperature.

Fig. 1: Polarized QCA Cells.

NML (NanoMagnetic Logic), despite QCA, uses nanomagnetic cells. These cells which are the base of the NML, perform signal propagation and logic by the interaction of magnetostatic field-coupling among them [3]. The cells when there is no external magnetic interference, tend to have their magnetization parallel to the longer axis of the rectangle as shown on Figure 2, with the purpose to minimize the magnetostatic demagnetizing energy. This configuration when pointing north-south or south-north has the same demagnetizing energy. NML uses these two states to associate as the '0' and '1' logic as a binary encoding.

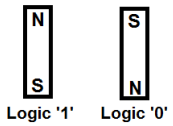


Fig. 2: NML magnetic cells.

The behavior of how NML transmits information is possible due to how magnetic interaction works. Like magnetic bars, the nanomagnetic cells have a fringing field that influences neighbor cells propagating information over the cells. It is important to note that the configuration side-by-side promotes nanomagnetic cells parallel one to another to be influenced with opposite polarity, i.e., if the first cells are polarized north-south, the second will be polarized south-north, the third north-south and so on. This configuration ended up creating one of the elementary logic gates: the inverter.

In this paper we propose the implementation of 3 adders in Nanomagnetic Logic that were previously implemented in Quantum Cellular Automaton analysing the difference between circuits designed in QCA and NML technology.

Section II shows more details about NML technology as well as the redesigned adders. Section III presents our methodology to redesign the adders. Section IV presents NML adders area results. Lastly, in Section V we present conclusion and future work.

II. Related Work

The NML has some special characteristics. It has a very low energy consumption to perform computation. It has a coplanar crossing of information, making it easier to create crossovers in NML circuits. NML also can work at room temperature. The only downside in these characteristics is the computation speed of NML circuits. They can only reach somewhere near 1 gigahertz, while CMOS transistor can reach far more speed than this.

Having only 3 clock zones, in comparison with QCA which has 4 clocks zones, also make the circuit signal easier to be propagated, but there is a recommendation that a wires length is 5 cells per clock, so that would be 5 cells in clock 0, 5 cells in clock 1 and 5 cells in clock 2 to create a wire with 15 cells.

In the NML technology there are two types of wire, the ferromangetic (Figure 3) and the antiferromagnetic (Figure 4). The ferromagnetic wire is always in the vertical, so the NML cells are in the same polarization along the entire wire. The antiferromagnetic is always in the horizontal, and the cells polarization are inverted cell by cell. This property of having cells polarization inverted depending on the cell position in the antiferromagnetic wire is used as the NML inverter.

The NML majority gate (Figure 5) is very similar to the QCA majority gates, having 3 inputs cells (A, B, and C) and one output cell (F). The 3 inputs are processed and available in the output cell. Depending on the input signals, the majority gate can work as an AND or OR logic gate.

Fig. 3: Ferromagnetic wire.

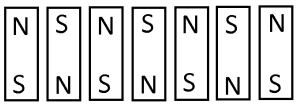


Fig. 4: Antiferromagnetic wire.

Fig. 5: NML Majority Gate.

Cho's adder [2] presents the best performance, because its layout is optmized to significantly reduce the signal delay propagation. It has 3 majority gates, 2 crossovers and 2 inverters in the 1-bit Cho adder, as shown in Figure 6a.

The adder proposed by Hänninen [4] is similar to Cho's adder, considering the number of majority gates and inverters is the same, but Haninen's adder has more cells and more crossovers, which causes a worse performance. Haninen's adder schematics is presented in the Figure 6b.

Zhang's adder [9] is an adder that uses a multi-layer strategy. It has 3 majority gates and 2 inverters, as we see in Figure 6c. Its performance is affected by the number of crossovers and the delay of the signal propagation, and the crossovers are multi-layered.

III. Methodology

Redesigning the adders from QCA to NML started by analyzing the schematic of each circuit, observing the inputs and outputs. To perform the redesign we have simulated the circuits and obtained the correct results as expected [8].

The adders were designed taking the QCA models as base and applying the NML characteristics to redesign the adders. One of the different characteristics of NML over QCA is the inverter. The signal inversion in NML is performed by having an even number of cells in an antiferromagnetic wire. Also, the signal cross in NML is made by a square shaped cells which cross the signals diagonally as shown in Figure 7, since in NML there is no multi-layer.

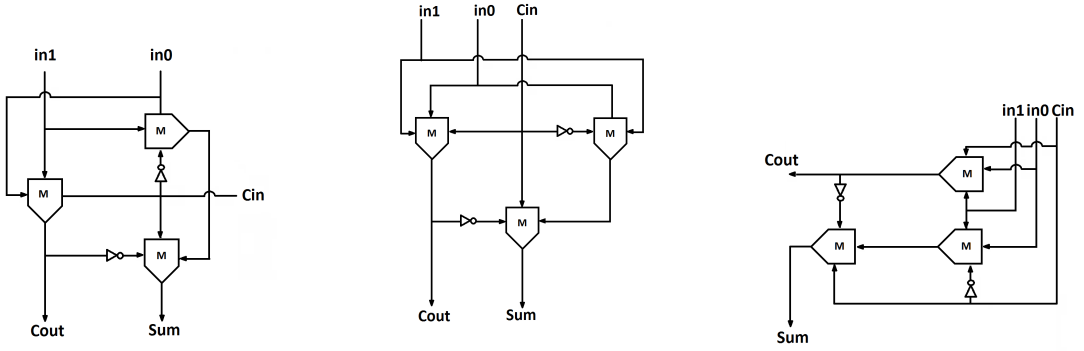
Considering these characteristics, we have analyzed the QCA adders [7] to perform the required modifications to fit in the NML restrictions, but also keeping the adders characteristics, such as the number of majority gates and crossovers. We couldn't keep the number of inverters because there is no inverter structure in NML, but whenever we needed to invert the signal, we used antiferromagnetic characteristic.

The first adder we redesigned was the Cho adder. It has 3 majority gates, 2 crossover and 2 inverters. Since the NML uses the number of cells in an antiferromagnetic wire to compose an inverter, we simply observed the majority and crossovers and built it as the schematic shows on Figure 8a. When we redesign the Cho adder in NML, the Cin signal spreads to the majority that calculates the Sum and we need to discard the first result that the Sum shows. After this modification the Sum and $Cout$ present the expected behavior.

The Hänninen adder follows the same idea as the Cho adder, since it has the same number of majority gates and inverters. The difference here is that Cho has one majority gate in the horizontal alignment and one less crossover (Figure 8b).

Zhang adder has the same amount of majority gates, crossovers and inverters as the Hänninen's adder but all majorities are in the horizontal alignment. This characteristic results in a layout that is very different from the previous two adders. Figure 8c shows this adder layout.

Each adder can be replicated to build wider adders, but we have to pay attention to the synchronization of the inputs and



(a) Cho Adder Schematic.

(b) Hänninen Adder Schematic.

(c) Zhang Adder Schematic.

Fig. 6: Corresponding schematics of the adders.

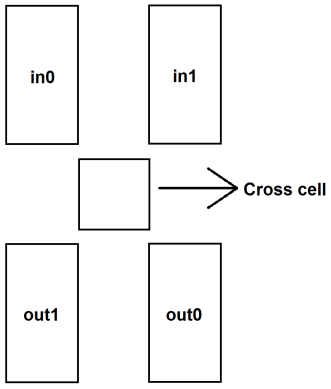


Fig. 7: Signal crossing in NML.

outputs. In Figures 9a, 9b, and 9c we have Cho, Hänninen, and Zhang 4-bit adders. In the Hänninen adders we needed to advance one clock zone on each extra adder so the outputs of each one could be synchronized with the inputs of the next adder.

IV. Results

One of the NML biggest advantages is the capacity to work at room temperature, because there are no considerable thermal effects. NML circuits have only 3 clocks, making it faster then QCA circuits, and NML has a very low energy consumption. Table I presents the area results for the implemented adders.

TABLE I: Comparison among area, width and length.

Adder	Area[a]	Width [b]	Length[c]
Hanninen	2.896.800 nm	1.420 nm	2.040 nm
Cho	1.917.600 nm	940 nm	2.040 nm
Zhang	5.374.600 nm	2.220 nm	2.430 nm

[a]The space between the cells is considered and was taken to 40nm between the vertical cells and 20nm between the horizontal cells.
[b]The cell width considered was 60nm.
[c]The cell length considered was 90nm.

The layout of Cho's and Hänninen's adders became quite similar as shown on Figure 8a and 8b respectively. This was caused because despite they have the same number of majorities and inverters, the disposal of the inputs and the crossovers make a great different in the layout, mainly because of the crossover and how it's implemented in the circuit.

V. Conclusions

In this paper we redesigned adders made in QCA to NML, taking in consideration the differences between the two technologies. Because of their differences, the circuits are not exactly the same in design, but their characteristics were maintained.

Possibilities for future works are the creation of a algorithm that maps the adder schematic in QCA and automatically redesign it to NML, an algorithm that automates the process of creating NML circuits in general and the study and creation of more NML circuits.

Acknowledgments

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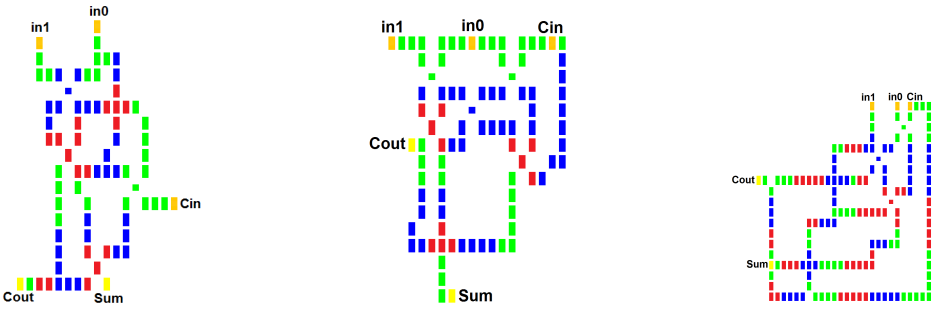
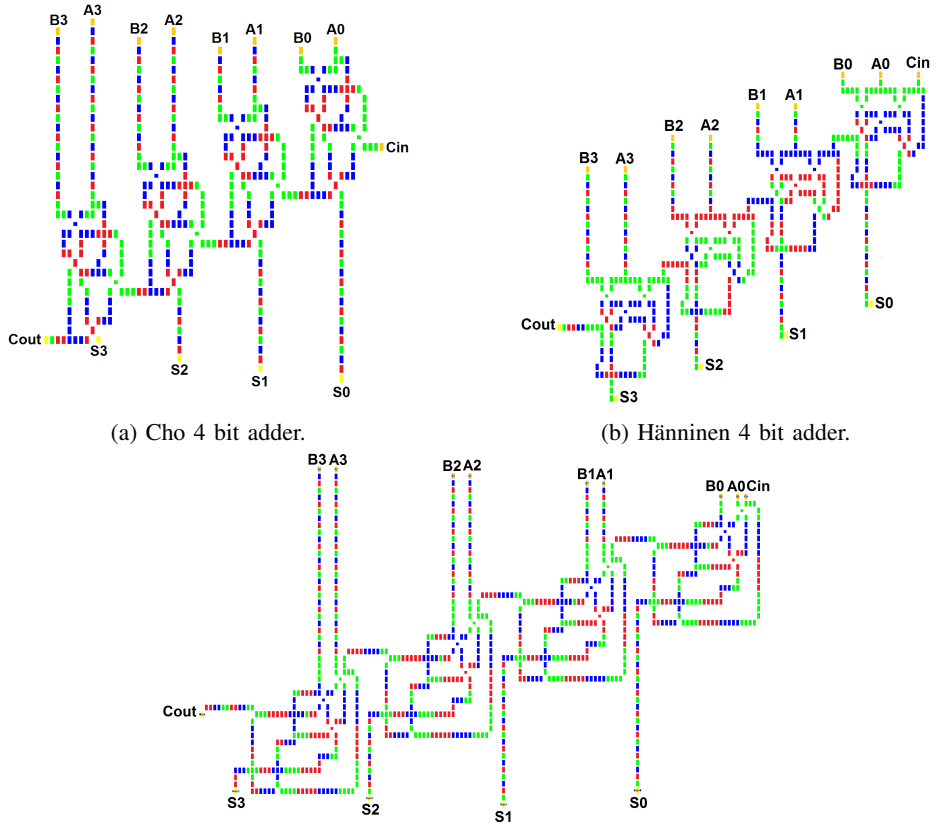


(a) Cho adder. (b) Hänninen adder. (c) Zhang adder.

Fig. 8: Corresponding adders in NML.



(a) Cho 4 bit adder.

(b) Hänninen 4 bit adder.

(c) Zhang 4 bit adder.

Fig. 9: Corresponding adders in NML.

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