Test Matrix for Schottky Diode Variability Characterization

Marcelo Pedrini, Thales Stedile Ribeiro and Yi Chen Wu
Under-graduate Students in Electrical Engineering, Federal University of Rio Grande do Sul,
Porto Alegre, Brazil
Email: marcelo.pedrini.br@gmail.com, thales2r@gmail.com, yichenpoa@gmail.com

Hamilton Klimach
Electrical Engineering Department, Federal University of Rio Grande do Sul,
Porto Alegre, Brazil
Email: hamilton.klimach@ufrgs.br
Sergio Bampi
PGMICRO and Informatics, Federal University of Rio Grande do Sul, Porto Alegre, Brazil
Email: bampi@inf.ufrgs.br

***Abstract*—In the nowadays very-low supply voltage applications, designers look around searching for circuit topologies and electronic devices that could operate in a satisfactory way also when under very low supply voltages. In this context Schottky diodes, that are usually employed only in electro-static discharge (ESD) protection circuits, could be a good option to substitute junction diodes, for example in bandgap voltage reference circuits (BGRs). Schottky diodes are available in any CMOS process, but foundries usually do not pay much attention on their characterization process because ESD circuits do not demand precise models. As a consequence the process design kit (PDK) information about Schottky diodes is very poor regarding variability data for mismatch and process simulation. This paper describes the development of an integrated Test Chip that could be used for statistical Schottky diode measurement and variability electrical characterization. It contains a matrix composed by four Schottky diode groups, each of them with one hundred devices of equal geometry. Each device is connected by MOS switches to the analog stimulus and measurement buses of a Semiconductor Device Parameter Analyzer, like the Agilent 4156 or B1500, that could be used for electrical voltage-current characterization. The MOS switches are controlled by a shift-register that is programmed through a serial digital bus by an external computer, which also controls the Device Analyzer programming the output voltages and measuring the diode current.**

Keywords*—*Schottky Diode, Variability Characterization, Test Circuit, CMOS.

I. INTRODUCTION

The progressive miniaturization of microelectronic circuits, beyond optimizing the use of silicon area and the speed of digital circuits, is also driven by its decreasing supply voltage (Vdd). The reason is that digital circuits supply voltage is directly linked to its power consumption, that is a critical factor to be taken into account by the designer in most current applications (dynamic power consumption is proportional to Vdd^2 in digital circuits). Beside that, low voltage operation is required for applications which make use of energy harvesting, an emerging technology that could be useful for the new Internet-of-Things (IoT) era [5].

However the operation with supply voltages below 1 V imply the need for new practical solutions for basic circuit topologies in analog and mixed-signal designs. A common example is a high performance voltage reference circuit that is an essential block for circuits like data converters, voltage regulators and phase-locked loops. The usual topology is the Bandgap Voltage Reference (BGR) and uses a PN junction diode as part of its main core, resulting that its minimal supply voltage is around 0.8 to 0.9 V. This limitation mainly occurs because the typical PN junction forward voltage is around 0.5 to 0.6 V for current densities sufficiently high to avoid errors when compared to leakage currents.

One possible solution to overcome this limitation would be the replacement of the PN junction by a metal-semiconductor junction [1], or Schottky diode, that presents a typical forward voltage around 0.2 to 0.3 V for a similar PN junction current density. Schottky diodes have been mainly used in protection networks against electrostatic discharges (ESD) and despite its widespread use, there is a lack of comportamental variability data about this device on PDKs given by the foundries. One explanation could be because usually there is no demand for detailed variability parameters in the design phase of this kind of application, since precise DC behavior is not a relevant aspect for ESD protection circuits.

But when using Schottky diodes as the main core of a voltage reference circuit, where low sensitivity to temperature changes and fabrication variability [2] are fundamental performance characteristics, besides the low sensitivity to power supply voltage, to current load and noise, the availability of more accurate variability parameters is fundamental in the design phase.

This work proposes an integrated Test Chip that can be used for electrical and thermal characterization of Schottky diodes, specifically regarding statistical variability measurement. It contains a device matrix composed by four Schottky diode groups, each of these groups with one hundred diodes of equal geometry. Each device of the matrix is connected to the analog stimulus and measurement buses of a Semiconductor Device Parameter Analyzer by MOS switches. The MOS switches are controlled by a shift-register that is programmed through a serial digital bus by an external computer, which also controls the Device Analyzer, programming the output voltages and measuring the diode current. The Semiconductor Device Parameter Analyzer could be an Agilent 4156, a B1500 or any other equipment with similar electrical voltage-current characterization functionality that offers at least two analog stimulus and measurement channels with force-sense feature.

This paper is organized as follows: after this introduction, chapter two presents some details about Schottky diodes, chapter three describes the diode matrix and chapter four shows the entire test circuit, including the layout of some critical parts. Chapter five presents simulation results and chapter six the final conclusions.

II. SCHOTTKY DIODE

The Schottky diode (named after German physicist Walter H. Schottky), also known as hot carrier diode, is a semiconductor diode formed by the junction of a semiconductor with a metal. It has a lower forward voltage drop and a faster switching action when compared to silicon diodes. A silicon diode has a typical forward voltage of 500 to 700 mV while the Schottky's forward voltage is around 150 to 450 mV [3],[6].

The main constructive difference between the Schottky diode and the PN junction diode is that the first one uses metal instead of the P-type semiconductor, but it is important to note that not every junction between metal and semiconductor makes a Schottky diode. Schottky diodes only happen when the contact is made with a weakly doped semiconductor. The forward biased Schottky diode voltage is strongly related to the type of metal used and to the junction quality, that is intimately related to the fabrication process.

The metal-semiconductor junction formed creates a Schottky barrier (instead of a semiconductor–semiconductor barrier as in conventional diodes). Typical metals used are molybdenum, platinum, chromium or tungsten, and certain silicides (e.g., palladium silicide and platinum silicide), whereas the semiconductor would typically be n-type silicon. The metal side acts as the anode, and n-type semiconductor acts as the cathode of the diode. In fact both n- and p-type semiconductors can develop Schottky barriers. However, the p-type typically has a much lower forward voltage being the usual choice.

Fig. 1 presents the comparison between the voltage-current behavior of Schottky and silicon PN diodes [3].

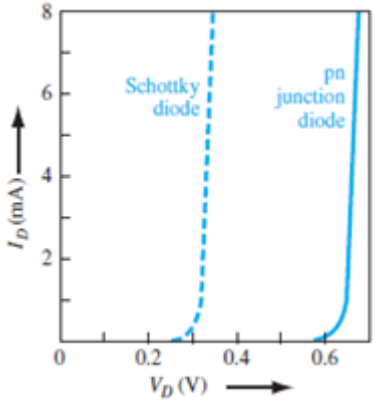

Fig. 1. *Comparison between VxI curves of both forward biased Schottky and PN junction diodes.*

The behavior of Schottky diodes can be described by Eq. 1 [3], where J is the junction current density, Φ_{Bn} is the barrier potential that depends on the device constructive details, A is the Richardson Constant that depends on electron mobility (which varies with semiconductor doping), T is the absolute temperature, V_a is the applied voltage, q is the electron charge and k is the boltzmann constant.

$$J = [AT^2 e^{\frac{-q\Phi_{Bn}}{kT}}][e^{\frac{qV_a}{kT}} - 1] \quad (1)$$

The Schottky diode physical structure can be made placing metal contacts directly over a weakly doped n-type semiconductor region, usually the n-well layer, forming the anode side. Since in the cathode side another junction is not desired, these metal contacts are placed over a strongly doped n-type diffusion layer. Fig. 2 shows the Schottky diode structure used in the IBM 130 nm process.

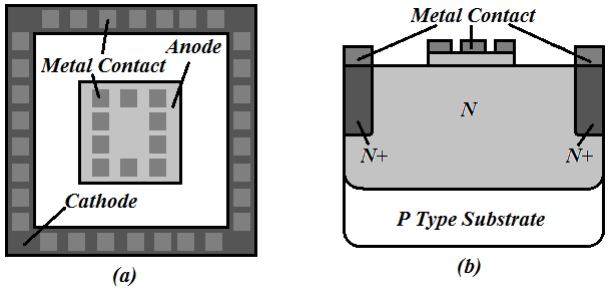

Fig. 2. *(a) Upper and (b) side views of the Schottky diode structure in the IBM 130 nm process.*

III. TEST MATRIX

The test matrix in this test chip is composed by 400 diodes divided in four groups of 100 each with same geometry, their sizes being 2μm x 2μm, 5μm x 5μm, 10μm x 10μm and 10μm x 10μm fingered. Each one of these 400 diodes is individually switched through MOSFET transistors that can connect any single device to the external pins of the integrated circuit (IC), which would be connected to the analog stimulus and measurement channels of the test equipment, usually a Semiconductor Device Parameter Analyzer. This topology provides the access to a large number of devices through a small quantity of external pins.

The test chip architecture needs the use of a test equipment that provides force-sense feature. The force-sense system sets the analog channel terminals with a certain voltage (or current) and estimates the resulting current (or voltage), ensuring the compensation of the resistive voltage drop on the stimulus path (connectors, contacts, wires, etc) that is surrounded by the sense feedback loop shown in Fig. 3, where *Rp* is the combined resistive effect of the MOS switch, wires and connections. The analog channel is then composed by two paths, the force path that excites the test node and the sense path that is responsible for measuring the effective voltage at the device terminals. This is the usually called four-wires or Kelvin measurement strategy.

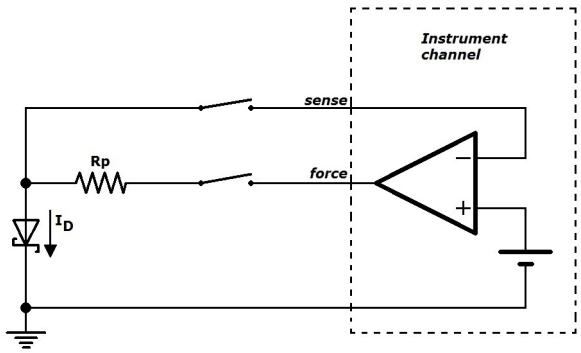

Fig. 3. *Force-sense measuring technique to avoid resistive drops in the stimulus path.*

IV. TEST CIRCUIT

The control of the switches that select the diode to be characterized, also named the device under test (DUT) that must be connected to the test equipment analog channels, is made through a serially loaded shift-register with a serial input *Din* and a clock control *Ck*. The shift-register is implemented with a group of 400 D-type flip-flops in serial cascade, being each one used to control a pair of MOS switches connected to the anode side of one diode. The *Qn* output activates the NMOS switch that connects the anode of the DUT to the *A-sense* channel path and the */Qn* activates the PMOS switch that connects the anode of the DUT to the *A-force* channel path, as presented in Fig. 4. When the shift-register is loaded with a certain 400 bit word, a pair of MOS switches is activated connecting the stimulus-measurement loop to the chosen device. A *Dout* signal pin is connected to the end of the shift-register to provide a verification way of the validity of the control word that was loaded in the last cycle. The *Din*, *Ck* and *Dout* digital signals are buffered to avoid rise or fall times degradation [4]. It should be noted that the cathode side of the diodes is connected to another force-sense channel using the *K-force* and *K-sense* pins to avoid resistive drops also.

The generation of the word to be loaded as well as the clock signal is done by an optically isolated digital interface board that is programmed by an external computer through the USB interface port. The computer also controls the test equipment, programming the stimulus voltage and measuring the resulting current. It also can control a thermal chamber, which allows the electrical characterization of the diodes in different temperatures. Fig. 5 shows the test setup architecture.

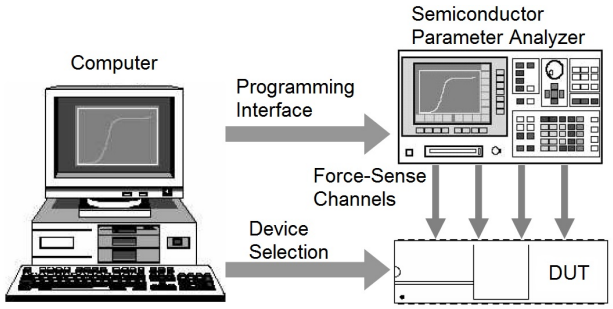

Fig. 5. *Test setup architecture composed by a computer, a Semiconductor Parameter Analyzer and the chip test that contains the DUTs.*

Many simulation situations were made with the diodes to evaluate the impact of the switches over the precision of the DUT electrical characterization. These results served as the basis to the definition of the switching topology (the way the MOS transistors are connected between the diodes and the analog channels) and the MOS switches geometries. After the connection topology was defined the simulation diodes VxI curves were used to the estimation of the PMOS transistors sizes, which are used to connect the force path.

The MOS switches were implemented with I/O-type transistors because they present higher operation voltage (2.5 V) and higher threshold voltage, resulting lower leakage currents when in the off condition. Table I presents the switching transistors dimensions related to the diode group geometry (the 'F' in the last geometry means that this group is composed by fingered diodes). The digital shift-register uses N and PMOS widths of 0.84μm and 1.68μm, respectively, and minimum length. Since the clock speed is very low the shift-register was implemented with static latches.

Table I. *Dimensions of the switching MOS transistors related to the diode group geometry.*

	PMOS			NMOS	
Diode Geometry	L	W	Fingers	L	W
$2\mu m$x$2\mu m$	$0.24\mu m$	$0.84\mu m$	1	$0.24\mu m$	$0.84\mu m$
$5\mu m$x$5\mu m$	$0.24\mu m$	$7.4\mu m$	5	$0.24\mu m$	$0.84\mu m$
$10\mu m$x$10\mu m$	$0.24\mu m$	$22.8\mu m$	10	$0.24\mu m$	$0.84\mu m$
$10\mu m$x$10\mu m$-F	$0.24\mu m$	$29.2\mu m$	10	$0.24\mu m$	$0.84\mu m$

V. SIMULATION RESULTS

The test circuit simulations were developed for forward voltages from 50 mV to 400 mV since this is the usual bias range of Schottky diodes, and were run for different temperatures since this test circuit could also be used to characterize the thermal dependency of the diodes. Fig. 6 presents the simulation curves of the four diode geometries obtained from just one diode (Diode LxW) and from the whole matrix (Matrix LxW) including the connection MOS switches, under typical temperature (300K or 27^{o}C). This graph reveals that accurate measurements can be done even the circuit having a great number of switches susceptible to current leakage.The only deviation that means inaccuracy occurs for the minimal diode geometry (2μmx2μm) and for bias voltages lower than 150 mV. Fig. 7 shows the IxV curves obtained from the 10μmx10μm diode simulations under 3 different temperatures: 225K (-48^{o}C), 300K (27^{o}C) and 400K (127^{o}C). Again the comparison between the diode curve alone and the whole matrix including the MOS switches can be done but now taking the temperature into account, showing that significant deviation occurs only for low voltages in low temperatures. Fig. 8 shows the basic cell layout composed by the P and NMOS transistors and the 5μmx5μm Schottky diode. After the cell layout is designed for each diode geometry it is regularly repeated to form the matrix since geometrical regularity improves the devices matching, that is an important factor in statistical characterization. Dummy devices were also included at the matrix borders to improve matching. The total area of the test circuit is 0.7x0.7 mm^2. The test chip will be sent for fabrication via MOSIS MEP program in the second semester of 2016.

VI. CONCLUSION

The supply voltage of some voltage reference topologies could be reduced if Schottky diodes were used instead of silicon PN junction diodes. The need for more accurate model parameters of Schottky diodes is the main motivation of this work, where a test matrix for Schottky diode variability characterization is presented. The proposed test circuit was designed to be implemented in the IBM 130 nm process and it contains a matrix composed by four Schottky diode groups, each of them with one hundred devices of equal geometry: 2μm x 2μm, 5μm x 5μm, 10μm x 10μm and 10μm x 10μm fingered. Each device is connected by MOS switches to the analog stimulus and measurement buses of a Semiconductor Device Parameter Analyzer, that is used for electrical voltage-current characterization. The resistive voltage drops over the switches, wires and connectors is compensated through a force-sense scheme. The MOS switches are controlled by a shift-register that is programmed through a digital bus by an external computer, which also controls the Device Analyzer programming the output voltages and measuring the diode current. The transistor switches were sized aiming for the best

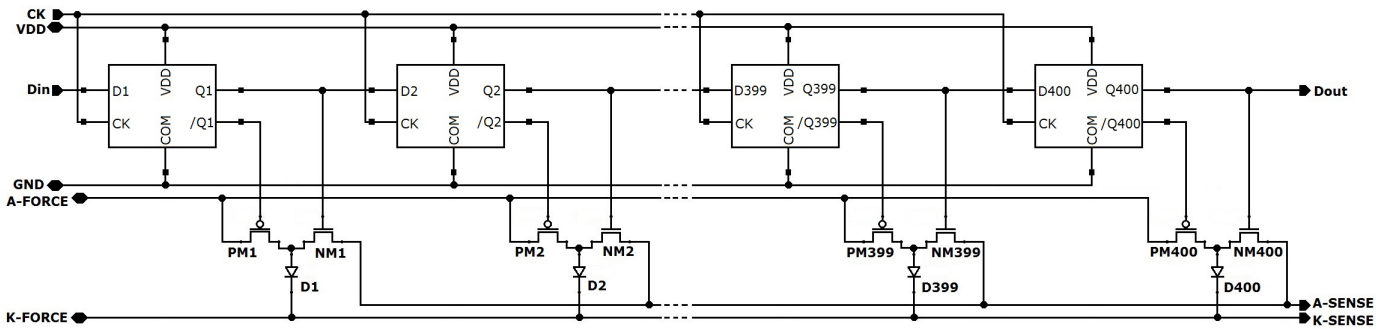

Fig. 4. *Shift-register and MOS switches connected to the diodes of the matrix.*

accuracy of the measurement under three temperatures: 225K, 300K and 400K. The whole matrix was simulated to evaluate the impact of the leakage of the switches in the diode current measurement accuracy. The total area of the test circuit is 0.7x0.7 mm^2. The test chip will be sent for fabrication via MOSIS MEP program in the second semester of 2016.

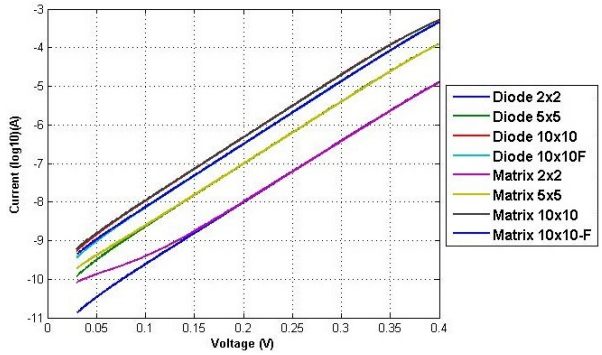

Fig. 6. *Comparison of the four diode geometries for just one diode (Diode LxW) and for the whole matrix (Matrix LxW).*

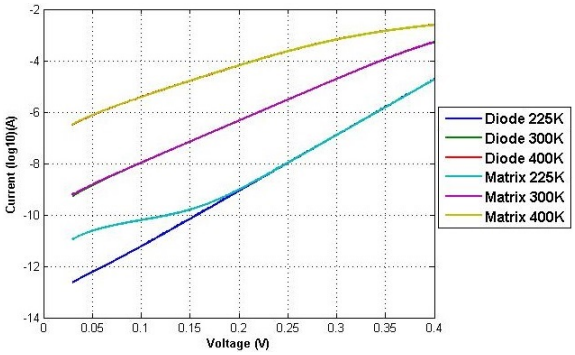

Fig. 7. *Curves from the 10μmx10μm diode, under 3 different temperatures, for the diode alone and for the whole matrix including the MOS switches.*

VII. ACKNOWLEDGMENTS

The authors are grateful to Propesq/UFRGS, Fapergs, MOSIS Education Program, CNPq and CAPES brazilian agencies, IC-BRAZIL Program and NSCAD Microelectronics.

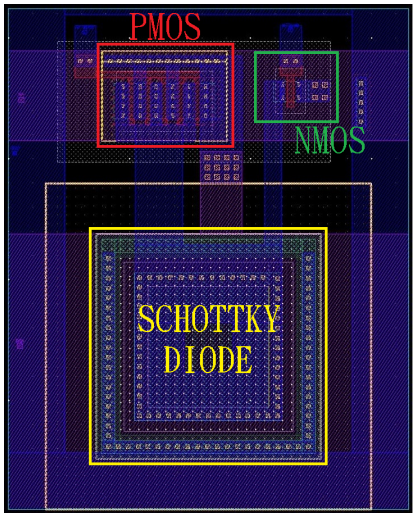

Fig. 8. *Layout of the P and NMOS transistor switches and the Schottky diode.*

REFERENCES

[1] Campana, R., Klimach, H. and Bampi, S. "0.5 V Supply Resistorless Voltage Reference for Low Voltage Applications," *In Proceedings of the 28th symposium on Integrated circuits and systems design (SBCCI)*, 2015, vol. 1.

[2] Mattia, O.E. "NanoWatt resistorless CMOS voltage references for Sub-1 V applications". *Dissertação de mestrado, PGMicro, UFRGS*, 2014.

[3] D.A. Neamen. *Semiconductor Physics and Devices*. McGrawHill, 4th edition, 2012.

[4] Klimach, H. "Mismatch model for MOS transistors". *Tese de doutorado, PPGEEL, UFSC*, 2008.

[5] Kinget, P. R. "Ultra-low voltage analog integrated circuits for nanoscale cmos". *Bipolar/BiCMOS Circuits and Technology Meeting*, 2007. BCTM '07. IEEE. [S.l.: s.n.], 2007. p. 144–148. ISSN 1088-9299

[6] Sze, Simon M.; Ng, Kwog K. *Physics of Semiconductor Devices*. Wiley-Interscience, 3th Edition, 2006.