# Design of a Didactic Chip for Study of the Basic Analog CMOS Building Blocks

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***Abstract*— This work describes the design of a didactic chip conceived in order to improve the understanding of the basic analog CMOS building blocks. Free tools were used for schematics capture, simulation, layout editing, extraction and verification. The chip contains different types of current mirrors, current adders, analog switches, differential pairs and basic amplifiers, which are briefly described. Some layouts are shown, as well as simulation results.**

***Keywords—Didactic chip; CMOS; Analog building blocks; Free EDA tools***

## I. INTRODUCTION

Despite the outstanding development on digital circuitry in recent years, analog circuits have a key role in electronic systems, especially when one considers the interfacing between digital systems and the real world, for which some kind of analog processing is frequently required. Therefore, it is worth to improve the education of the analog engineer with methodologies that are, at same time, motivating and technologically well structured.

The courses related to Analog Electronics (and their support bibliography) emphasizes currently the study of topologies well suited for integrated implementation, such as the polarization by current sources (realized by current mirrors) and use of differential pairs [1]. However, the laboratory realization of these structures is quite difficult and impractical, if discrete components are used. Because of this, a gap can be observed between the theoretical study of these blocks and their experimental verification.

This project describes the design of a didactic chip conceived in order to study the basic building blocks of an analog CMOS integrated circuit (IC). Didactic chips are reported in the literature, as in [2–4]. It can be noted that, although it is virtually impossible to address all the blocks (due to die size and pin count limitation), each didactic chip prioritize some types of topologies. However, in the two cited references, there is a goal to let the undergraduate or graduate students to bias, configure and test blocks by themselves, getting an appropriate insight about analog integrated circuits.

The work was developed at the Federal University of Juiz de Fora – UFJF, during an undergraduate scientific initiation project. An important fact is that free Electronic Design Automation (EDA) tools were used. Besides the cost issues, the motivation for the use of free apps was their faster learning curve and easier installation procedures, if compared to most of the commercial platforms. Moreover, these tools were better suited to the still reduced number of researchers involved in the area of Microelectronics in UFJF, currently in its initial stage.

The main blocks are reported in Section II, while the layout and simulation of some of the building blocks are described in Section III. The main conclusions and future works are presented in Section IV.

## II. DESCRIPTION OF THE BUILDING BLOCKS

The chip is composed by a set of basic building blocks of an analog CMOS IC, as follows: (i) current mirrors, based on *n*-channel MOSFETs – NMOS and *p*-channel MOSFETs – PMOS, in different topologies; (ii) common source amplifiers (NMOS and PMOS), with active loads; (iii) source follower (NMOS only); (iv) common source amplifier cascaded by a source follower; (v) differential pairs (NMOS and PMOS); (vi) current adders (NMOS and PMOS); and (vii) analog switches (CMOS, NMOS and PMOS). Most of these structures are explained in [5], and their design in this work is briefly described in the following items.

### A. *Current mirrors*

There are sixteen NMOS mirrors, and the same number of PMOS mirrors. All the mirrors have two outputs. The reasons for it are: (a) to compare the mismatch between the input and *one* of the output currents (which is intrinsically related to the output impedance of the mirror topology); (b) to compare the mismatch between the *two* outputs, since some mirrors were laid out intentionally unmatched, for comparison with their counterparts designed under well-known matching techniques; (c) to construct additional current processing schemes.

In order to allocate a reasonable variety of blocks without exceeding the pin count of the chip, all the current mirrors of same type (NMOS or PMOS) share the same pins, by means of

an analog multiplexer. This uses analog CMOS switches to convey the input/output currents into the selected mirror, as described in Fig. 1. The switches are selected by a 4-to-16 line decoder, designed with adapted standard cells from a free library, available in [6]. The decoder is the only one digital block of the chip.

The parameters of the mirrors are described in Table I. Each NMOS mirror of the table has a PMOS counterpart with same features.

### B. *Common-source amplifiers, source follower and common-source cascaded by a source follower*

A common-source amplifier with an active load, often referred as an analog inverter with active load [5], is used typically as the second stage of the classic Miller Operational Transconductance Amplifier (OTA), and has a high theoretical relevance. This block is included in order to be studied separately from any other. Two versions are available: one using a NMOS and one using a PMOS as the amplifier element.

An independent source follower amplifier was included (NMOS only), as well as a common-source stage cascaded by a source follower, in order to let the students to compare the DC, AC and transient responses of these structures.

### C. *Differential pairs*

The differential pair is a fundamental building block, since it is encountered at the first stage of any OTA or operational amplifier. Three differential pairs were designed: a simple NMOS differential pair, a simple PMOS pair and a cascode PMOS pair. They were designed to be biased with 40 µA.

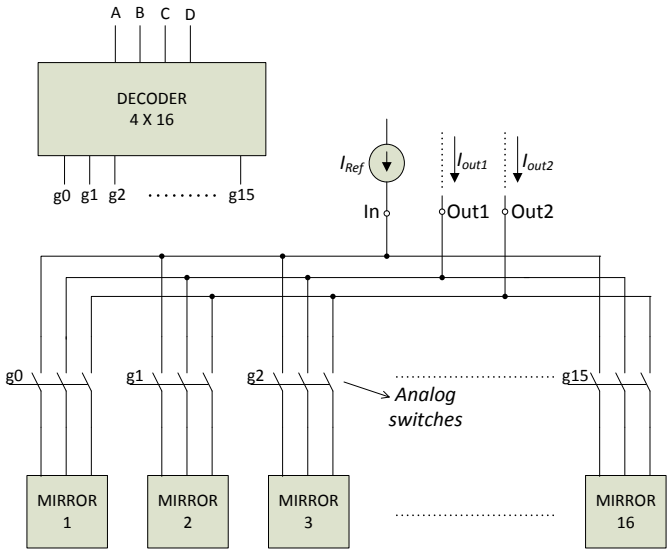



Fig. 1. Current mirrors mutiplexing scheme.

TABLE I. PARAMETERS OF THE CURRENT MIRRORS.

| Mirror No. | Parameters | | |
|---|---|---|---|
| | Topology | Rating (µA) | Matching |
| 1 | Basic | 40/40/40 | Matched |
| 2 | Basic | 40/40/40 | Unmatched |
| 3 | Basic | 40/80/80 | Matched |
| 4 | Basic | 40/80/80 | Unmatched |
| 5 | Basic | 80/80/80 | Matched |
| 6 | Basic | 80/80/80 | Unmatched |
| 7 | Basic | 80/160/160 | Matched |
| 8 | Basic | 80/160/160 | Unmatched |
| 9 | Wilson | 40/40/40 | All Matched |
| 10 | Cascode | 40/40/40 | |
| 11 | Cascode | 80/80/80 | |
| 12 | Cascode | 80/160/160 | |
| 13 | Modified Wilson | 40/40/40 | |
| 14 | Modified Wilson | 80/80/80 | |
| 15 | High compliance | 40/40/40 | |
| 16 | High compliance | 80/80/80 | |

### D. *Current adders*

There are two current adders, based on NMOS and PMOS devices. The PMOS-based current adder is shown in Fig. 2. It can be seen that it use the cascode configuration, in order to give a high output impedance. With these structures, it is possible to plan several practices emphasizing the current-mode analog processing.

### E. *Analog switches*

There are four analog switches: NMOS, PMOS and two CMOS. All the switches share one pin, and are controlled by the first four output lines of the 4-to-16 decoder. With these switches, it is possible to elaborate practices regarding the properties of analog switches.

## III. LAYOUT, SIMULATION AND VERIFICATION

The chip was designed within the ON Semi C5N Process (5-V, 0.5-µm, NWELL, triple metal, analog CMOS). The initial SPICE simulations were performed using a free model available in [7]. Refined simulations were made using the BSIM4 models available from ON Semi through MOSIS, by the assignment to a MEP (MOSIS Educational Program) research account.

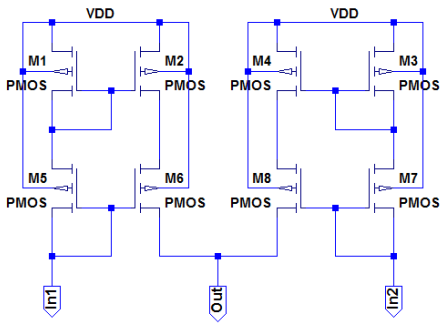



Fig. 2. A PMOS current adder.

The LTSpice IV software, provided by Linear Technology, was used for the simulations. It is a free and intuitive SPICE simulation platform, without node limits restriction.

The Electric VLSI Design System is used for the layout, due to its free access and fast learning curve. Moreover, it has the MOSIS Scalable (SCMOS) design rules built-in, which are used in the project [8]. Several chips designed with Electric and effectively sent for fabrication are reported in the literature, as in [9, 10], for example. The LVS checking was done by using Netgen, a Linux-based tool [11].

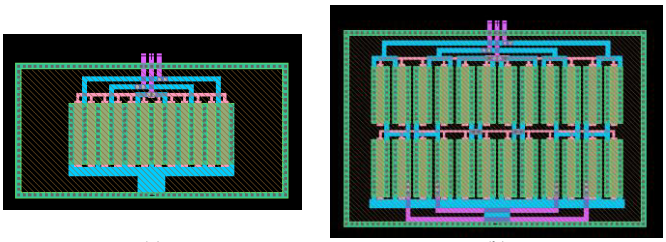
DC sweep, AC sweep and transient analysis were performed for each block, as it can be illustrated by the following examples.

### A. *Current mirrors*

The layouts of the current mirrors 1 (basic, 40/40/40 µA, matched) and 10 (cascode, 40/40/40 µA, matched) are shown in Fig. 3. A DC sweep was performed in LTSpice IV, from a netlist extracted from the layout, given by Electric. The plot of the output current against the terminal output voltage is shown in Fig. 4 for the two mirrors. In both examples, the input current was 40 µA and all MOSFETs have W = 16.2 µm and L = 1.8 µm, with multiplicity factor M = 4.

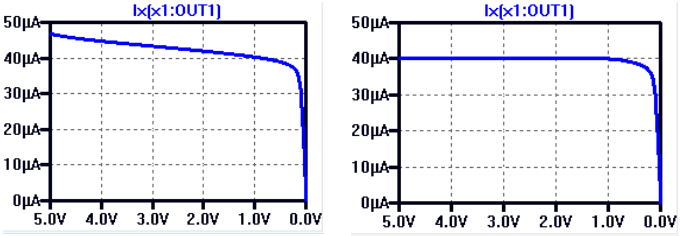
### B. *Common source amplifier*

The common source amplifiers with active loads were laid out together with the source follower and the differential pairs, in two general analog blocks: one of them contains the NMOS devices and the other one contains the PMOS devices, as illustrated in Fig. 5.



(a) (b)

Fig. 3. Layout of two NMOS current mirrors. (a) Simple mirror, 40/40/40 µA, matched; (b) Cascode mirror, 40/40/40 µA, matched.




(a) (b)

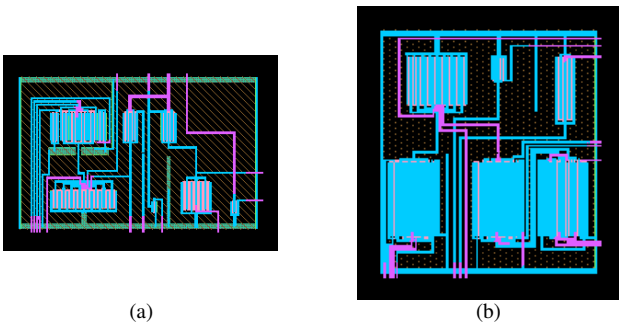
Fig. 4. DC sweep simulations of the output current versus the output voltage for the mirrors of Fig 3. (a) simple mirror; (b) cascode mirror

The schematic of the NMOS common source amplifier (with PMOS active load) is illustrated in Fig. 5, with external biasing resistors and decoupling capacitor, and a load of 32 pF // 10 MΩ, which represents a typical oscilloscope probe, added to some stray capacitances. For $M_1$, W/L = 9 µm/1.2 µm (M = 2); for $M_2$, W/L = 45 µm/1.8 µm (M = 4). The biasing current was 40 µA.

An AC analysis for this circuit was performed, leading to the plot on Fig. 6. It can be noted that, even without an output stage, the response of this circuit can cover almost the entire audio bandwidth. Then, it can be used in any practice that handles with signals with frequencies up to approximately 18 kHz. The gain in the bandwidth is 41 dB.

A transient simulation for this same circuit is depicted in Fig. 7, for an input signal with amplitude 10 mV and frequency 1 kHz. The output signal has amplitude close to 1.1 V.

For a common-source amplifier cascaded by a source follower, whose elements are also embedded in the two general analog blocks, it is possible to boost the bandwidth to approximately 2 MHz, for the same load.



(a) (b)

Fig. 5. Layouts of the general analog blocks. (a) NMOS; (b) PMOS.

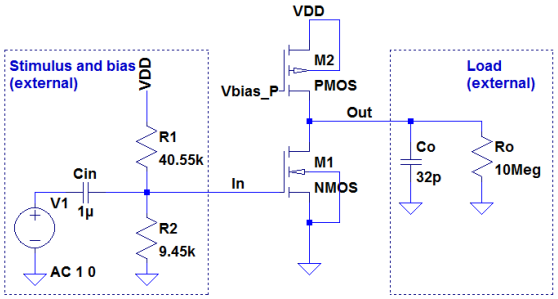



Fig. 6. Schematic of the NMOS common source amplifier (PMOS active load), with external elements.

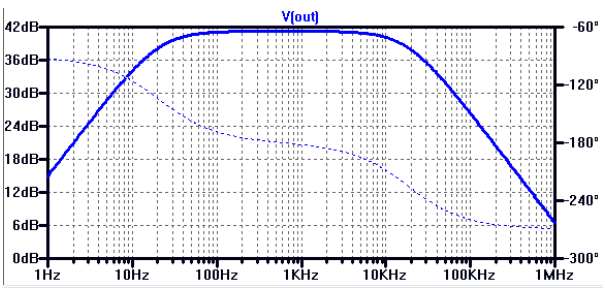



Fig. 7. AC simulation of the NMOS common source amplifier.

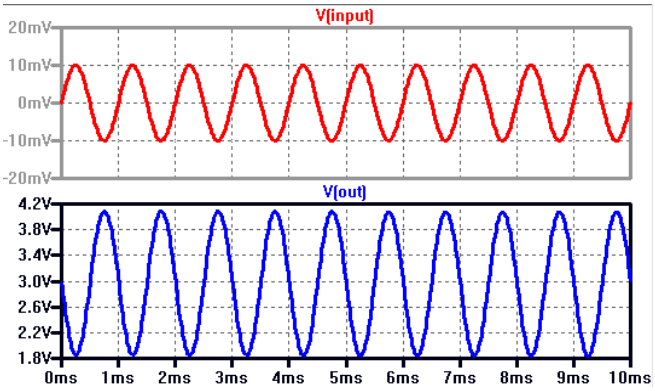



Fig. 8. Transient simulation of the NMOS common source amplifier: input signal (top) and output voltage (bottom).

### C. *Layout of the chip*

The layout of the entire chip is displayed in Fig. 9, with indication of its main blocks, identified as follows: 1 – PMOS mirrors; 2 – NMOS mirrors; 3 – 4-to-16 line decoder; 4 – analog switches of the mirrors multiplexers; 5 – general purpose analog switches; 6 – PMOS current adder; 7 – NMOS current adder; 8 – general analog blocks (contain the common source amplifiers, source followers and differential pairs). The padframe was adapted from a library available in [7].

The die size is 2.4 x 2.4 mm (chip area of 5.76 mm$^2$), and the planned packaging is LCC52 (52 pins).

## IV. CONCLUSIONS

This work described the design of a chip conceived to study the basic building blocks of the analog CMOS circuits. The objective is to shorten the existing gap between the theory and practice regarding the fundamentals of analog integrated circuits, allowing a variety of activities for undergraduate or even graduate students.

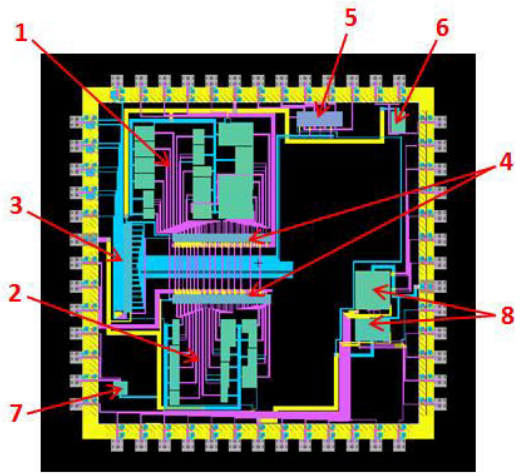



Fig. 9. Chip layout, with indication of its main blocks: 1 – PMOS mirrors; 2 – NMOS mirrors; 3 – 4-to-16 line decoder; 4 – analog switches of the mirrors multiplexers; 5 – general purpose analog switches; 6 – PMOS current adder; 7 – NMOS current adder; 8 – general analog blocks.

Free EDA tools were used for schematic editing, simulation, layout, extraction and DRC/LVS verifications. Along the development of the project, these tools have proven to be suitable for the design of a small to medium sized chip in a 0.5-µm standard CMOS technology, especially if considering a scientific initiation project.

It is expected that the chip can be further manufactured using the MOSIS service, by means of the educational account.

Once fabricated, the chip will be assembled in a development board containing jumpers, switches, biasing resistors and the other elements that could enhance the interfacing with the laboratory instruments.

The Laboratory of Electronic of the Engineering College of UFJF – LABEL has purchased a number of National Instruments ELVIS II kits, employed in the analog and digital electronics classes. With this platform, it is possible to test the chip, by performing DC and AC characterization, besides the measurement of the time-domain responses. In other words, the simulations mentioned as examples in the Section II can be effectively conducted in practice, and many other didactic activities can be planned.

## ACKNOWLEDGMENTS

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