Comparative Analysis of Parasitic Resistance Extraction Methods Applied to FinFETs

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***Abstract* – In this paper, a comparative analysis of three parasitic resistance extraction methods when applied to FinFETs is presented. The methods of Terada and Muta, Hu et al. and Dixit et al. are considered. The parasitic resistance was extracted from drain current as a function of gate voltage curves, obtained from three-dimensional numerical simulations. The parasitic resistance was analyzed for different fin widths and doping concentrations at source and drain regions. Terada and Muta and Hu methods showed very similar results, both in absolute values and trends. Dixit method presented the most different absolute values, but it was consistent regarding to the parasitic resistance trends.**

Keywords—FinFET; Parasitic Resistance; Extraction Method.

I. INTRODUCTION

FinFETs are a promising alternative to continue the evolution of semiconductor devices in nanometric scales, thanks to their narrow fin width (W_{FIN}) and multiple gate structure that allow a better coupling and decreasing short channel effects [1] [2]. However, the thin structure imposes a high source and drain resistance (R_{PAR}), which degrades the drain current [3]. The decrease of R_{PAR} is one of the requirements to allow the continued scaling process on these devices [4]. For this reason, it is very important to know the R_{PAR} values, to be sure that the proposed alternatives for its reduction can be quantified and modeled in a reliably way. There are no consolidated methods for the extraction of the parasitic resistance in nanometric devices, most of them were proposed for conventional MOS devices. The aim of this work is to evaluate three R_{PAR} extraction methods when applied to FinFETs: Terada and Muta method [5], Hu et al. method [6] and Dixit et al. method [7].

II. DEVICE SIMULATION

Three-dimensional simulations were performed in Atlas Simulator [8]. Fig. 1(a) shows the FinFET structure as generated in Atlas, indicating the dimensional variables. The gate wraps three surfaces (laterals and top) of the silicon fin, but the thick oxide layer in the top, called hard mask, avoids the formation of the inversion channel in the top. The inversion channels are formed just in the lateral surfaces, reason why this device is considered as double gate. Fig. 1(b) shows the total current density in a cutplane located at $H_{FIN}/2$. Notice that in the channel region the current is concentrated in the silicon/oxide interface. In the source and drain extension regions (L_{EXT}) the current distribution is quite uniform, while below the silicide (L_S) the current is more concentrated at the beginning of silicide and diminishes along L_S. Table I presents the simulated devices characteristics, which were defined according to experimental devices studied in [9], [10] and [11]. The drain current as a function of gate voltage curves for a low drain voltage bias (V_{DS} = 50 mV) were used to extract R_{PAR}. The threshold voltage (V_T) of all devices is 0.4V.

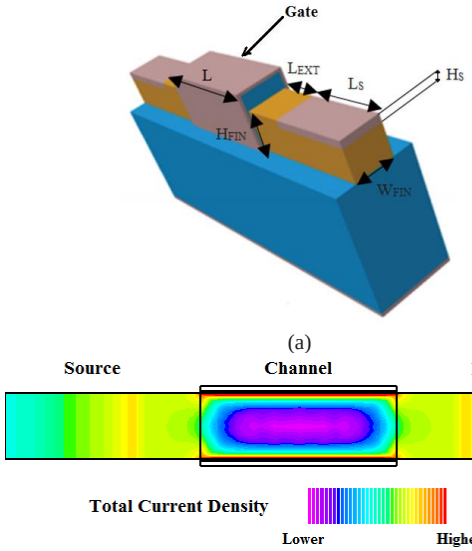

Fig. 1. (a) Three-dimensional structure of the simulated FinFET and (b) Total current density in a cutplane located at $H_{FIN}/2$.

TABLE I. SIMULATED DEVICES CHARACTERISTICS

Variable	Symbol	Value
Channel length	L (nm)	150, 175 and 200
S/D extension length	L_{EXT} (nm)	50
S/D contact length	L_S (nm)	100
Fin width	W_{FIN} (nm)	30, 40, 50 and 60
Fin height	H_{FIN} (nm)	50
Silicide Thickness	H_S (nm)	10, 15, 20, 25, 30, 35 and 40
Channel doping concentration (p-type)	N_A (cm^{-3})	$1x10^{15}$
S/D extension doping concentration (n-type)	N_{DEXT} (cm^{-3})	$1x10^{19}$
S/D-HDD doping	N_{DHDD} (cm^{-3})	$1x10^{19}$ and $5x10^{19}$
Contact resistivity	ρ_S ($\Omega.cm^2$)	$1x10^{-7}$
Gate oxide thickness	t_{ox} (nm)	2
Hard Mask Thickness	t_{HM} (nm)	20

III. PARASITIC RESISTANCE EXTRACTION METHODS

In this section, the three studied methods will be presented, in order to understand their origin and how to use them.

A. *Terada and Muta Method [5]*

Terada and Muta developed one of the most known methods for the R_{PAR} extraction in 1979. With this method it is possible to determine the effective channel length in MOSFETs and also distinguish the values of the resistance of source and drain regions. It is a graphic method that uses the total resistance (R_{TOTAL}) curve as a function of the channel length (L) in the linear operation

region for gate biases above the threshold voltage. The R_{PAR} value is extracted at the point where the lines cross to each other, i.e. the only point independent of V_G, showing that the channel resistance was separated from source and drain resistance. Fig. 2 shows an example of extraction for a FinFET using this method.

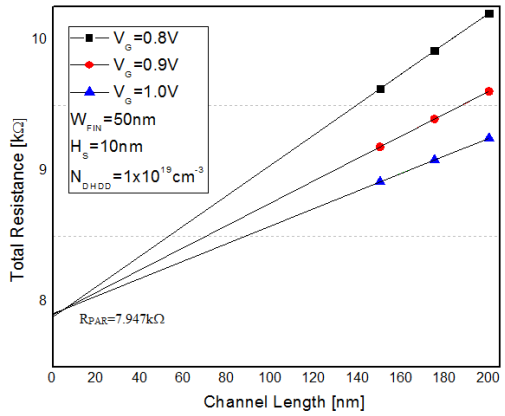

Fig. 2. Example of R_{PAR} extraction method using Terada and Muta method.

B. *Hu et al. Method [6]*

Hu J. et al. proposed another method of extracting parasitic resistance, in 1987. For them, the R_{PAR} is dependent on the gate voltage. For this reason, two voltages V_{G1} and V_{G2} of the gate with very close values are used and for a given gate voltage V_{GX} two straight lines are obtained one for each voltage obtained through the equations (1) and (2):

$$V_{G1} = V_{GX} - \frac{\Delta V_G}{2} \quad (1)$$

$$V_{G2} = V_{GX} + \frac{\Delta V_G}{2} \quad (2)$$

From these calculated voltages, an examination of R_{TOTAL} as a function L when operating in the linear region. Analogously to Terada and Muta method, the intersection between the two curves shows the R_{PAR} value obtained. The lower the value of V_G, the better the solution provided by this intersection lines. Fig. 3 presents an example of this method for a FinFET. The authors also declare that their method is valid for devices with Lightly Doped Drain (LDD) regions, unlike Terada and Muta method.

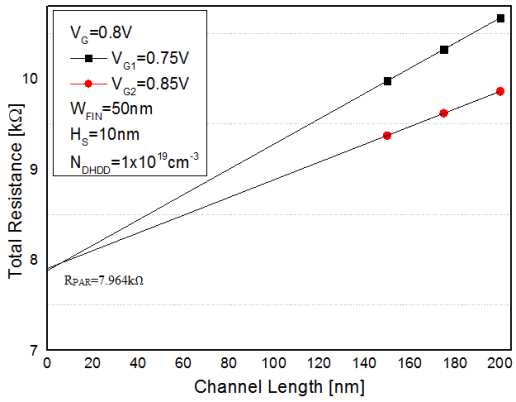

Fig. 3. Example of R_{PAR} extraction method using Hu, et al. method.

C. *Dixit et al. Method [7]*

In 2005, Dixit et al. proposed a method also known as first order exponential method. According to the authors, the methods mentioned above were unable to capture the source resistance and drain from the narrowing of these regions and the current conduction in different crystallographic planes. The method involves the analysis of an exponential curve adjusted to the R_{TOTAL} curve as a function of gate voltage (V_G) when the device operates in the linear region, generating the asymptote of the curve. For high V_G values, R_{TOTAL} becomes constant, becoming the value of R_{PAR}. Fig.4 shows an example of extraction from this method for a FinFET, the parasitic resistance was extracted for V_G = 5V.

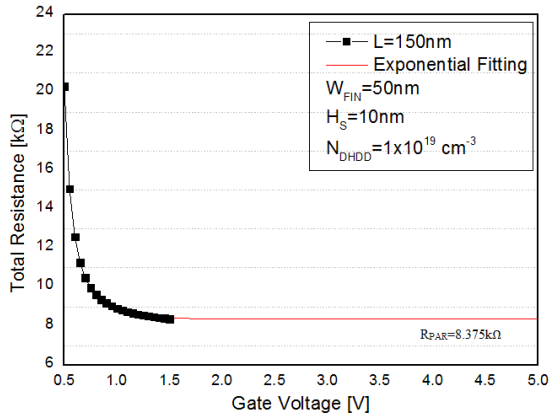

Fig. 4. Example of R_{PAR} extraction method using Dixit et al. method.

IV. Results and Discussion

The first analysis was made for devices with the same doping concentration at the source and drain regions (N_{DEXT}=N_{DHDD}=1x10^{19} cm^{-3}) and W_{FIN}=50nm. Using Terada and Muta method, V_G of 0.8; 0.9 and 1V for the calculation of R_{TOTAL} were used. The R_{PAR} values were obtained for different silicide thicknesses (H_S), as shown in Table II and Fig. 5. Notice that the R_{PAR} values decrease as H_S increases until H_S=30nm, due to the increase of the lateral contact area, i.e., the cross section of the silicide. For thicker silicide films, the path below the silicide becomes throttled, and R_{PAR} increases with H_S from this point.

TABLE II. R_{PAR} VALUES FROM TERADA AND MUTA METHOD.

H_S [nm]	R_{PAR} [kΩ]
10	7.947
15	7.762
20	7.630
25	7.564
30	7.564
35	7.649
40	7.858

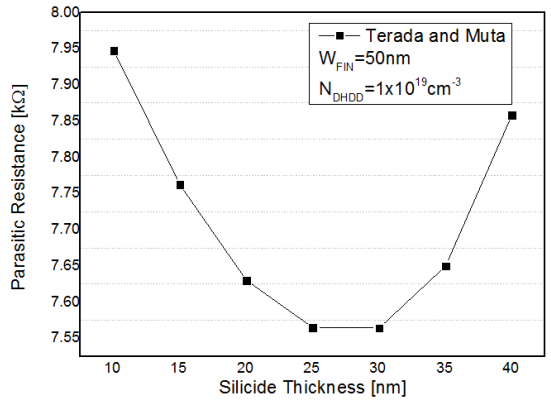

Fig. 5. R_{PAR} x H_S graphic obtained using Terada and Muta method.

In the simulations using Hu method, for comparative purposes, we used the same gate polarizations, with "step" (ΔV_G) equal to 0.1V. From the equation model provided by Hu, we obtained V_{G1} and V_{G2}. The obtained R_{PAR} values are shown in the table III and Fig.6.

TABLE III. R_{PAR} VALUES OBTAINED USING HU METHOD.

H_S [nm]	R_{PAR} [kΩ] V_G=0.8V	R_{PAR} [kΩ] V_G=0.9V	R_{PAR} [kΩ] V_G=1.0V
10	7.964	7.940	7.948
15	7.777	7.731	7.738
20	7.677	7.627	7.600
25	7.584	7.580	7.562
30	7.580	7.554	7.539
35	7.664	7.661	7.629
40	7.887	7.853	7.840

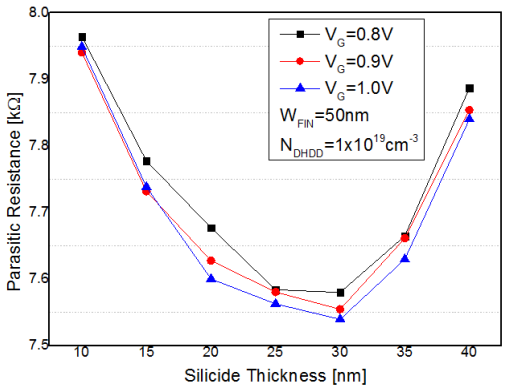

Fig. 6. R_{PAR} x H_S graphic obtained using Hu method.

It can be seen that the results are very close to those obtained using Terada and Muta method, we can observe the same trend, varying more significantly for higher gate polarizations. In order to evaluate the reliability of Hu's method in LDD devices, simulations were performed for a device with such structure, with $N_{DHDD}=5x10^{19}cm^{-3}$. The results are shown in table IV and Fig.7. We can observe that the R_{PAR} behavior in LDD devices using the Hu method is very similar to that obtained in devices that do not have this structure.

TABLE IV. R_{PAR} VALUES USING HU METHOD FOR LDD DEVICES.

H_S [nm]	R_{PAR} [kΩ] V_G=0.9V
10	6.677
15	6.540
20	6.436
25	6.375
30	6.368
35	6.420
40	6.580

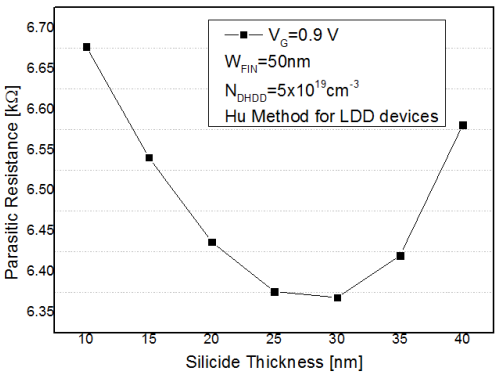

Fig. 7. R_{PAR} x H_S using Hu method for LDD devices.

For Dixit method, the results for different L are shown in table V and Fig. 8. It can be observed that the parasitic resistance has differences in the numeric values but the same trend of the previous studied methods. As the source and drain regions of the three devices has the same characteristics, the R_{PAR} values should be the same for the three channel lengths, with shows that the exponential adjust can add errors to R_{PAR} values.

TABLE V. R_{PAR} VALUES OBTAINED USING DIXIT METHOD.

H_S [nm]	R_{PAR} [kΩ] L=150 nm	R_{PAR} [kΩ] L=175 nm	R_{PAR} [kΩ] L=200 nm
10	8.375	8.365	8.444
15	8.190	8.269	8.348
20	8.061	8.175	8.300
25	7.992	8.071	8.189
30	7.990	8.069	8.148
35	8.075	8.154	8.233
40	8.285	8.365	8.444

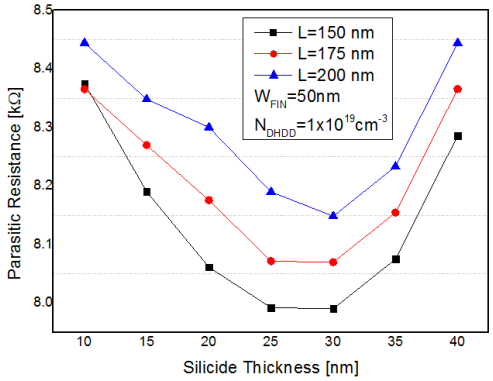

Fig. 8. R_{PAR} x H_S graphic obtained using Dixit method.

Dixit also claims that the previous methods cannot extract precisely the value of the resistance for narrow fin devices. Therefore, for comparative purposes, simulations were performed for different W_{FIN} and H_S= 25nm, shown in table VI. We can observe that the value of R_{PAR} varies significantly, decreasing with W_{FIN} increase, which was expected as the source and drain areas become lower.

TABLE VI. R_{PAR} VALUES OBTAINED USING DIXIT METHOD FOR DIFFERENT W_{FIN} VALUES.

W_{FIN} [nm]	R_{PAR} [kΩ] L=150 nm	R_{PAR} [kΩ] L=175 nm	R_{PAR} [kΩ] L=200 nm
30	13.355	13.525	13.695
40	10.334	10.516	10.688
50	7.992	8.071	8.189
60	7.318	7.484	7.649

Fig. 9 shows the comparison obtained from the different methods, for structures without LDD (9a). We can observe the same trend in all of them, with greater variation obtained in Dixit method. This difference is probably due to differences in the application method, since we are dealing with linear extrapolations and exponential curves. To verify the affirmation about LDD devices in Hu's article, in Fig. 9b and Table VII the R_{PAR} values were also extracted from Terada and Muta and Dixit methods. It is noted that all three methods gave similar results. Hence, the use of LDD devices does not invalidate Terada and Muta method in these devices. The obtained results show that even for LDD devices the value of R_{PAR} obtained using Terada and Muta method shows a very similar behavior of Hu method, where R_{PAR} x H_S curves are overlapping. Dixit method shows a similar tendency to the previous simulation, having lower R_{PAR} values.

TABLE VII. R_{PAR} VALUE OBTAINED USING TERADA AND MUTA METHOD AND DIXIT METHOD IN LDD DEVICES.

H_S	R_{PAR} [kΩ] Terada and Muta	R_{PAR} [kΩ] Dixit L=175 nm
10	6.682	7.807
15	6.544	7.668
20	6.438	7.566
25	6.380	7.505
30	6.368	7.493
35	6.422	7.547
40	6.581	7.711

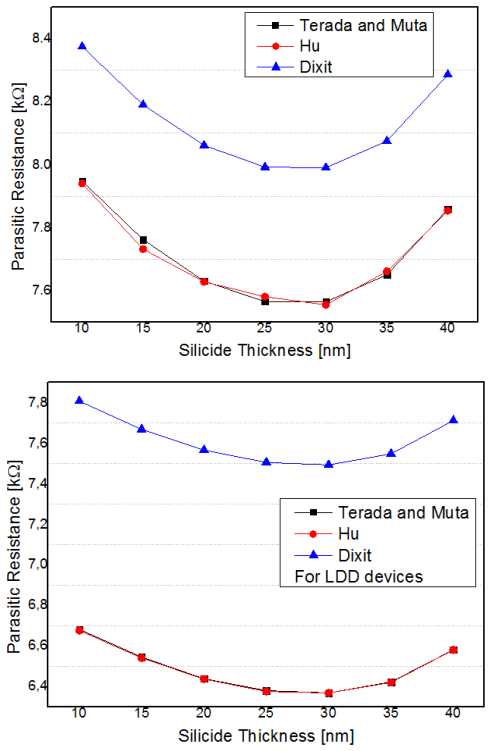

Fig. 9.a) Comparison of the three methods for devices: a) without LDD and b) with LDD.

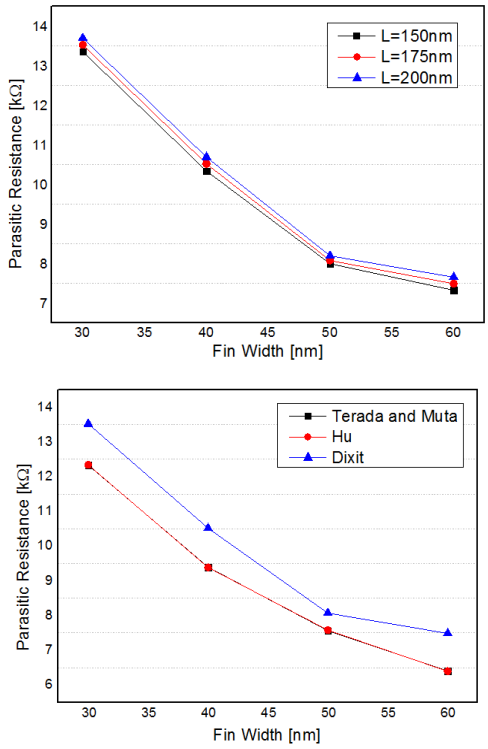

Fig. 10.a) R_{PAR} x W_{FIN} graphic obtained using Dixit method and b) Comparison for the three different methods for different W_{FIN} values.

Extractions were also made for Terada and Muta and Hu methods for H_S=25nm to verify Dixit's claim that his method is more effective in extracting the source and drain series resistance from the narrowing of these regions. The results are shown in Table VIII and in figures 10 a) and b). We can see that the values obtained using Dixit method, regardless of narrowing the fin width, are slightly larger doesn't having a larger discrepancy compared to other methods when W_{FIN} decreases. Therefore, the narrowing of the fin does not invalidate the use of the methods of Terada and Muta and Hu in these devices. For all methods, the extracted R_{PAR} values are compatible with experimental values for devices with such source and drain characteristics [3], showing that the three dimensional simulation performed in Atlas can be reliably used to analyze R_{PAR} of FinFETs. As a future work, the comparison between the absolute values obtained from the different methods can be inserted in circuit simulators to study the impact of the different R_{PAR} values in the drain current of devices.

TABLE VIII. R_{PAR} VALUES OBTAINED USING TERADA AND MUTA AND HU METHODS FOR DIFFERENT W_{FIN} VALUES.

W_{FIN}	R_{PAR} [kΩ] Terada and Muta	R_{PAR} [kΩ] Hu
30	12.336	12.343
40	9.395	9.386
50	7.564	7.580
60	6.399	6.395

V. CONCLUSIONS

This paper focused on three methods of parasitic resistance extraction: Terada and Muta, Hu, J et al. and Dixit, A et al. By applying these methods to FinFETs, and analyzing the R_{PAR} values, we can see that the methods of Terada and Muta and Hu did not present significant differences in their results. Comparing the previously mentioned methods with Dixit, the difference between their values becomes more evident. Hu et al said that their method was developed to be used both in conventional devices as in LDD devices, and, from the analysis of data obtained in the simulations, it was noticed that all three methods gave similar results. Therefore, the use of LDD devices does not invalidate the other methods. Dixit et al claims that the previous methods cannot extract R_{PAR} for narrow fin devices, therefore, for comparative purposes, simulations were performed for different W_{FIN}, and the three methods presented the same trends, invalidating such affirmation. In general, it could be observed through the different methods of extraction that their numerical values varied, but there is a consistency regarding to the trends, independent of the different analyzed characteristics.

ACKNOWLEDGMENT

The authors would like to thank Centro Universitário da FEI, FAPESP and CNPq for the financial support.

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