Temperature and Wavelength Impact in Lateral PIN SOI Photodiode's Current with Second Interface Bias

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***Abstract*— Lateral PIN photodiodes have many applications, such as optical communication, security systems, gas detection and classification, medical equipment and space observation. This paper studies the substrate polarization influence, alongside with the light and temperature influence on the lateral PIN SOI (*Silicon-On-Insulator*) photodiode.**

***Keywords*— PIN Photodiode; SOI; Temperature.**

I. INTRODUCTION

Lateral PIN photodiode sensors constructed using the SOI technology operating in hazards applications, such as spatial environments, can suffer interference from temperature variation that can lead to problems in device's response. Based on that, their behavior must be fully understood in order to be correctly predicted and circumvent such problems. The use of numerical simulators is widely spread and is a very useful approach, because many of the phenomena studied, such as the interference of the temperature and the incidence of different electromagnetic radiation wavelengths cannot be observed internally without the aid of TCAD numerical simulators. The numerical simulations studied in this paper are based on experimental devices from Université Catholique de Louvain (UCL) [1] and they returned the device behavior in conditions variating the temperature, polarization and wavelength of incidence light.

II. THE SOI PIN PHOTODIODE STUDIED

The SOI technology is composed by a silicon oxide layer under the active silicon layer, known as buried oxide, that separates the device from the substrate. The buried oxide reduces parasitic effects caused by radiation [2]. The lateral PIN SOI photodiode (Fig. 1) is composed of anode (P+), intrinsic (P-) and cathode (N+) regions.

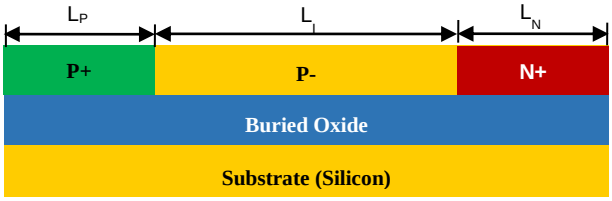

Fig. 1. Lateral PIN SOI Photodiode representation.

Two-dimensional numerical simulations of the lateral PIN SOI photodiode were performed using the numerical simulator Sentaurus Device TCAD, from Synopsys [4]. The numerical simulation models match the initial mobility, recombination and electric field of the experimental devices from UCL [1]. The device has P+, I and N+ regions with length of 4.5µm, 8µm and 4.5µm, respectively. The active silicon layer has thickness of 80 nm and the buried oxide thickness is 400 nm [5].

The length of the depletion region (RDD) can vary until its maximum length according to the voltage applied between P+ and N+ regions. When the diode is in the direct polarization state, the diffusion current overcomes the drift current, and then the RDD region decreases. When in the reverse polarization state, the drift current overcomes the diffusion current, and then the RDD region increases. With the bias of the substrate, it is possible to control the operation mode of the intrinsic region through the second interface that can vary among accumulation, depletion and inversion states [3].

Two wavelengths are adopted to study the influence of different penetration depth. They are: 397nm and 465nm. Additionally, five temperatures ranging from 300K to 500K are numerically simulated to analyze its influence on the device behavior.

III. RESULTS AND DISCUTIONS

Below, will be introduced the studied topics and the results obtained in this work.

A. Operation Modes Study

The curves below were obtained in dark condition, at 300K. With these curves was possible to see the operation modes and was possible to analyze the carriers (holes and electrons) behavior over the device in each operation mode.

The Fig. 2(a) introduces the cathode current curves ($I_{cathode}$) as a function of substrate voltage with six anode biases (V_{anode}), they are: -0.25V, -0.50V, -0.75V, -1.00V, -1.25V and -1.50V. The Fig. 2(b) introduces $I_{cathode}$ as a function of anode voltage with eight substrate biases, they are: -20V, -10V, -6V, -2V, 0V, 2V, 6V and 10V.

In Fig. 2(a), it is possible to identify the regions of: accumulation mode for substrate biases lower than about -5V, inversion mode with substrate bias higher than about 0V and depletion mode with substrate bias between -5V and 0V. For lower anode biases, there are lower substrate biases and higher cathode current, due the increase of the depletion length.

During the accumulation mode, occurs the cathode current decrease, the electron mobility decrease and the rise of recombination because of the high hole concentration. When the cathode current rises abruptly, and the recombination increase significantly, there is the depletion mode. During the inversion mode, the minority carriers are responsible for the drift current and the majority carriers are responsible for the diffused current. In this case, the device is not illuminated, and the electron concentration is higher than hole concentration, the inversion cathode concentration is larger than the accumulation cathode current.

In Fig. 2(b), it is possible to observe the low and virtually constant cathode current (between 10^{-10}µA e 10^{-9}µA) for negative substrate biases. The Inversion occurs with 0V anode bias and, from this point, it is possible to see the cathode current growth (maximum value $I_{cathode}$=10µA).

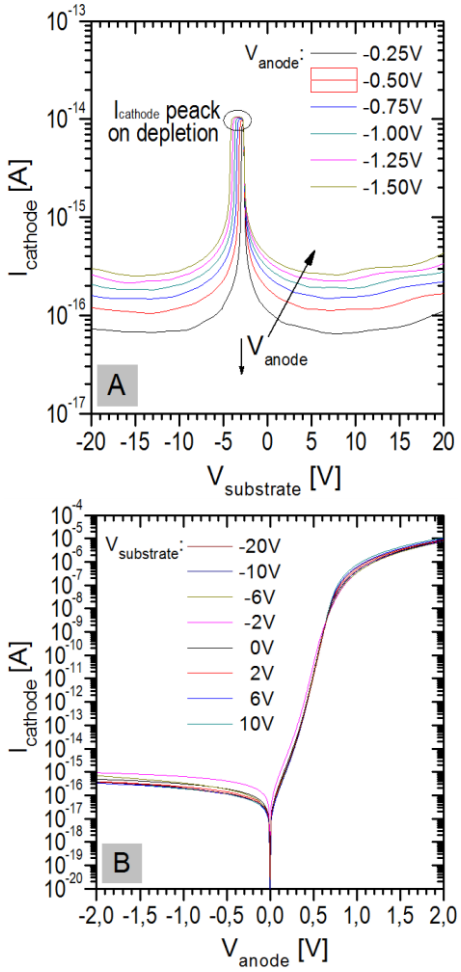

Fig. 2. Cathode current as a function of (a) substrate voltage with different anode polarizations and (b) as a function of anode voltage for different substrate polarizations.

Electron and hole concentrations along the diode length, 1nm below the top and 1 nm above the bottom of the silicon active region, were extracted from the simulated devices with -0.25V and -1,5V anode biases, as presented in Fig. 3. The -20V and +20V substrate biases represent the accumulation and inversion modes, respectively. For the depletion mode, it was selected the substrate bias which occurs in the peak of each cathode current curve.

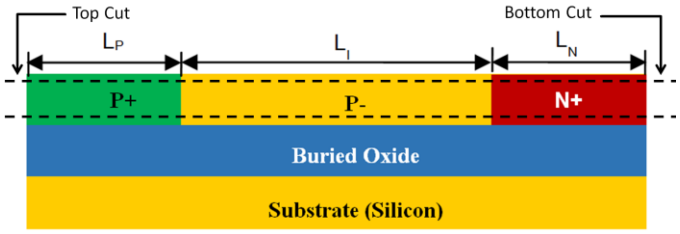

Fig. 3. Lateral PIN SOI Diode cuts representation.

The Fig. 4 (a) and (b) represents electron concentrations while Fig. 5 (a) and (b) represents hole concentrations. In Fig. 4 and 5 can be observed the regions of the device. In the P+ type region there is a large hole concentration, while in the N+ type region there is a large electron concentration.

With the negative substrate bias applied, the device is in accumulation mode and the holes are accumulated in the bottom of the device and the electrons are pushed to the top of the device. It is also possible to observe that, in the depletion mode, the hole and electron concentrations are similar in the top and bottom regions.

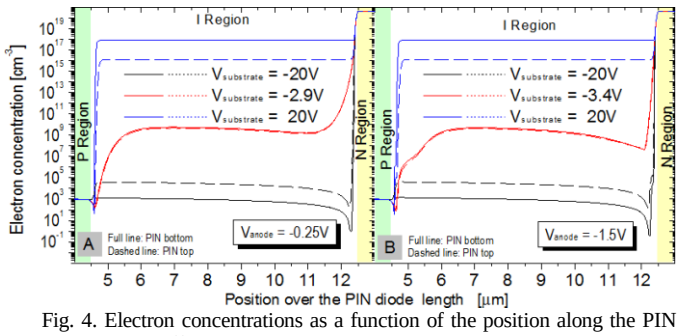

Fig. 4. Electron concentrations as a function of the position along the PIN diode length with different substrate biases.

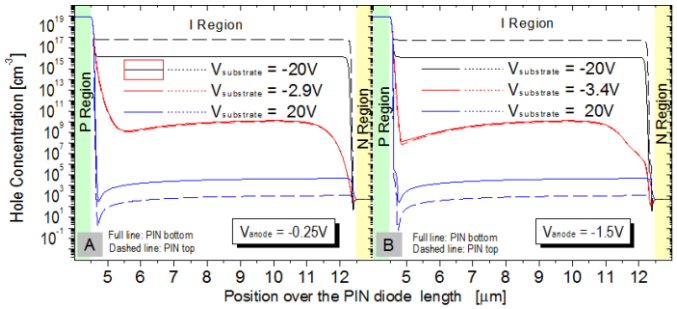

Fig. 5. Hole concentrations as a function of the position along the PIN diode length with different substrate biases.

B. Light and Temperature Influence

The light and temperature influence will be discussed in this topic. The curves below were obtained for two different wavelengths (397nm and 465nm) and at five different temperatures (300K, 350K, 400K, 450K and 500K). Figure 6 (a) and (b) presents the cathode current ($I_{cathode}$) as a

function of substrate voltage, for six anode biases (V_{anode}) and illuminated with two wavelengths: 397nm (Fig. 6 a) and 465nm (Fig. 6 b). It is also possible to identify the three operation modes described before.

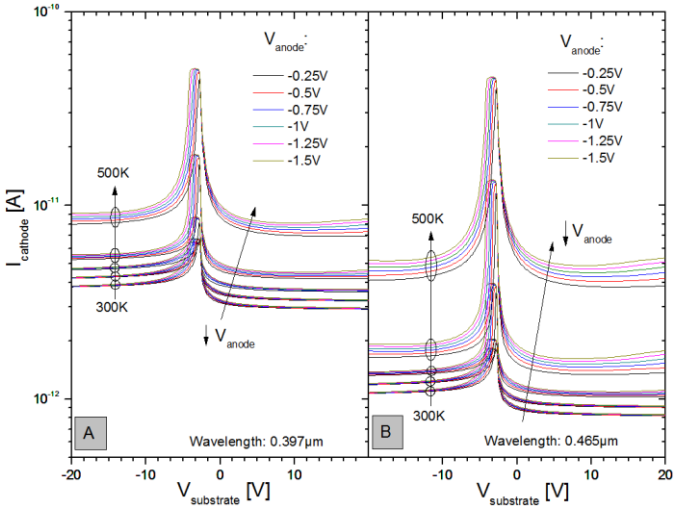

Fig. 6. Cathode current as a function of substrate voltage for wavelengths of (a) 397 nm and (b) 465 nm.

It is worth to note that the photodiode simulated here is composed by one single finger, while in practical applications of photodetectors the multifinger structure is implemented to increase the photogenerated cathode current.

Notice that the substrate bias for the maximum depletion peak didn't change because of the SOI technology, which isolates the active silicon region from the substrate, but for higher temperatures, there are higher cathode currents. The temperature rise causes the dark current rise, however small is the increase of the dark current, harm the device performance and increase the noise.

Observe that, for the higher temperature (500K), the inversion cathode current is larger than accumulation cathode current, instead of the other temperatures. As known, during the inversion mode, the minority carriers are responsible for the drift current, the majority carriers are responsible for the diffused current and the total current is the sum of the diffused current and the drift current. In temperatures high enough, the diffused current will surpass the drift current, so the inversion cathode current will be larger than accumulation cathode current. For the other temperatures, the drift current is larger than the diffused current.

With the diode reversely biased and illuminated, electron-hole pairs generated in the RDD region are separated by the electric field and collected by anode and cathode before the recombination, increasing the total current. Comparing figures 6 (a) and (b), it is possible to see the light wavelength influence on the cathode current. The light incidence increases the cathode current due to the electron-hole pairs generated and captured by the P+/N+ regions and, for low wavelengths the cathode current is higher than to larger wavelengths [6].

If the penetration depth surpasses the thickness of the silicon active region, 80nm in this case, part or total of the incidence light will reach the buried oxide, then the quantum efficiency, responsiveness and precision of the device will be compromised. Due to this characteristic, the correct wavelength must be selected for the device in accordance to the active silicon layer thickness.

Observing the Fig. 7 (a) and (b), it is possible to notice that the cathode current minimum occurs for different anode voltage values, due to the temperature influence and light incidence that results on optical generation, rising the diffused current and the needed anode bias to occurs the depletion.

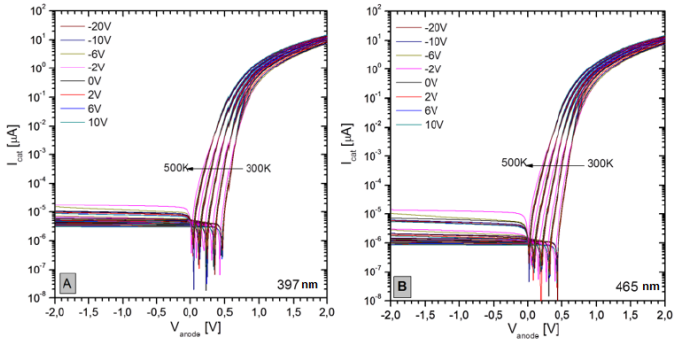

Fig. 7. Illuminated cathode currents for two wavelengths of (a) 397 nm and (b) 465 nm, as a function of anode voltage.

In the Fig. 7 (a) and (b), notice that for different operation temperatures, the dark current is affected, as well as the diode performance. The increase of temperature rises the dark current by several orders of magnitude, as a result of increased thermal generation of electron-hole pairs [2]. Observing the temperature influence in the Fig. 7 (a) and (b), it is possible to see that higher temperatures lead to higher cathode currents due to thermal generation.

As a large dark current is considered an undesired characteristic in a photodetector, constituting a background noise in photodiode sensors, it is possible to affirm that the quantum efficiency, responsiveness and precision of the device will decrease with the temperature growth as it increases the dark current.

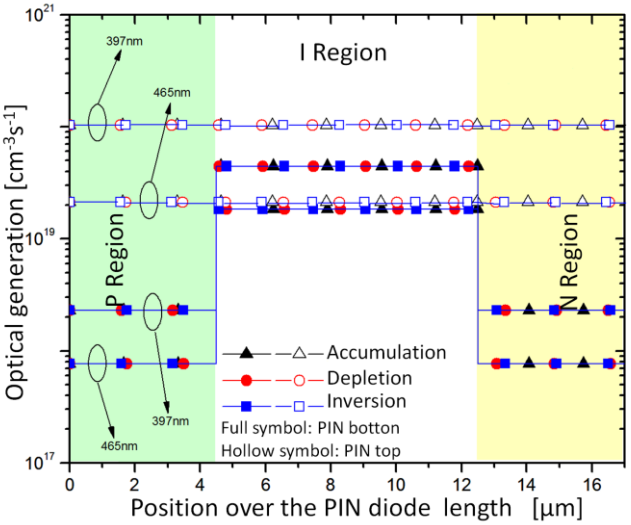

Fig. 8. Optical generation as a function of the position over the PIN diode length with different biases, wavelengths and temperatures.

Observing the Fig. 8 it is possible to see again that for the wavelength of 397nm the cathode current is higher than for the wavelength of 465nm, due to the fact that part of the photons from the 465nm wavelength trespasses the active silicon layer. Also, it is important to highlight that all the different temperatures curves are overlapping, indicating that the temperature does not interfere significantly the optical generation.

IV. CONCLUSIONS

Analyzing all the curves, it is possible to observe the different diode operation modes: accumulation, depletion and inversion. Also was noticed the substrate bias difference for the maximum depletion for different anode bias and the larger electron concentration in the top of diode and the larger hole concentrations in the bottom with negative substrate biasing. The incidence of light and the rise of temperature affect the device performance. Due to the shorter penetration depth of the shorter wavelength, most of the electron-hole pairs generated are inside the active region of the diode, increasing the cathode current, opposed to the longer wavelength, where most part of the photons trespasses the active silicon region of the device.

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