Exploring Alternative Designs of Majority Voters

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***Abstract*— Due to transistor shrinking, devices are more sensitive to faults in nanotechnologies. In contrast, many applications need to ensure a high level of reliability. Hardware redundancy remains the most adopted technique to deal with radiation effects, mainly the triple redundancy technique (TMR). However, the critical part of a TMR system is the majority voter. Alternative architectures are proposed in the literature for improve the robustness of this block. It is important to know the characteristics of each alternative to identify the best candidate for each design. In this context, this work evaluates performance and power characteristics of seven majority voter architectures at 32nm technology and provides a study about the voltage variability effects on the expected behavior of investigated voters topologies.**

Keywords— majority voters, variability, nanotechnology

I. INTRODUCTION

The evolution of computers and electronic devices follows the progress of integrated circuits (ICs) through the technology scaling, resulting in higher transistor density, higher complexity, and higher manufacturing defects probabilities. Because of these effects, yield and reliability are becoming a major concern in IC design [1]. Manufacturing defects are the main source of permanent faults. Permanent faults are always present in the circuit due to manufacturing process and can also be caused by aging effects.

The field of fault tolerance faces the challenge of keep an acceptable level of service of a system, even in presence of faults [2]. Fault tolerant techniques are implemented to deal with this issue. A widely used fault tolerant technique is the Triple Modular Redundancy (TMR). It consists in an architecture composed of three identical modules performing the same function and a majority voter [3]. The idea behind the TMR is that a defective module propagating an error can be masked for the two other fault-free modules and can guarantee a full masking to a single fault. A majority voter is responsible for voting the correct output. Clearly the voter is the weak point for fault tolerance. In the last years, several majority voter architectures were proposed in the literature to enhance the robustness of this TMR component [5-8]. Although, there is a lack of works that evaluating these architectures designed in the same conditions about timing and power consumption at 32nm technology node.

In this context, the main goal of this work is to evaluate performance and power characteristics of different majority voter topologies at 32nm technology and provide a study about the voltage variability effects on the expected behavior of investigated voters architectures.

This paper is organized as follows: Section II presents seven different implementations of majority voters evaluated in this work. Section III describes the methodology and circuit structure used to evaluate the voters. Section IV presents the results and finally, section V presents the final remarks.

II. MAJORITY VOTERS

In a TMR system, the majority voter compares the output of each module bit-by-bit to vote the correct output. The majority voter function has three inputs (“A”, “B” and “C”) and one output S, and decide the output by majority as showed in the corresponding canonic Boolean expression is given in Eq. 1. All possible combinations of inputs for the majority voter are shown in TABLE I.

$$S=AB+AC+BC \quad (1)$$

TABLE I MAJORITY VOTER TRUTH TABLE

A	B	C	S
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

In this work, seven majority voter architectures are explored [4-8] and the circuits are presented in Fig.1. The most conventional implementation is the CMOS logic gate, named CLASSICAL voter [4] and presented in Fig. 1(b). The main advantage of this implementation is the low number of transistors involved. However, its structure is considered less robustness to faults. The CLASSICAL voter is mainly used in studies to compare with other majority voter architectures.

The NAND voter and NOR voter, illustrated in Fig. 1(c) and (d), are the Eq. (1) implemented through NAND and NOR gates respectively. Both are implemented with 18 transistors. Another topology used in this study is the one proposed by [5] with 30 transistors, the KSHIRSAGAR voter, shown in Fig.

1(f). It is a proposed fault-tolerant voter based in a priority encoder that selects the outputs to a multiplexer to implement the majority function. This circuit was design to tolerate stuck-at and transient faults.

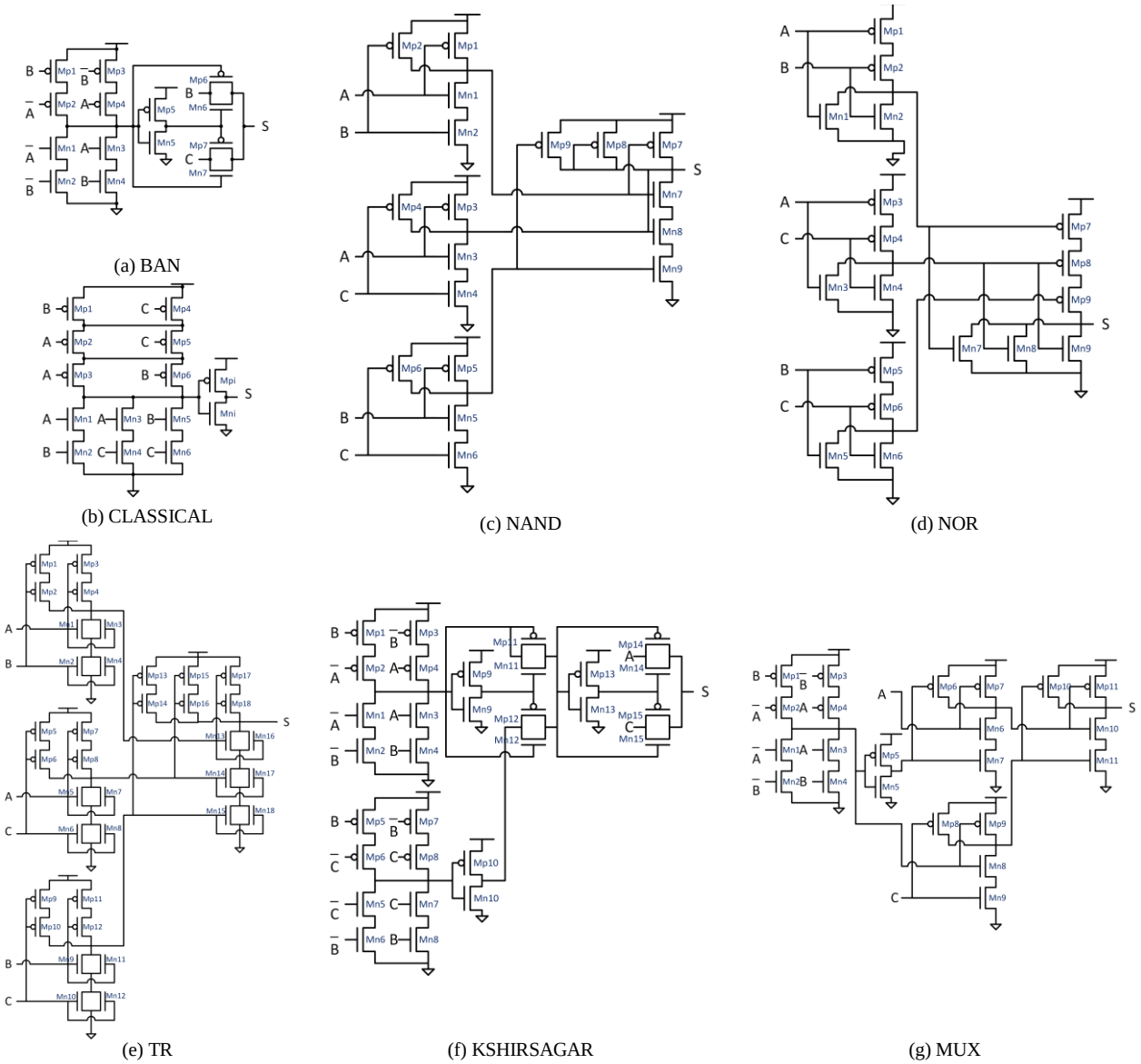
The BAN voter, shown in Fig. 1(a) is a simplification of the KSHIRSAGAR circuit. According to [6], a voter with less transistors has lower probability of having a fault. Therefore, the main advantage of the circuit is the reduced power consumption and area, since it was implemented with 14 transistors as the CLASSICAL. Another proposed fault-tolerant voter based in a multiplexer is the MUX [7], shown in Fig. 1(g). This implementation is similar to BAN circuit, but the multiplexer is implemented through NAND and inverter gates, having a higher number of transistors.

The last majority voter analyzed in this work is the TR voter, shown in Fig. 1(e). It uses transistor redundancy for shielding the NAND-NAND or NOR-NOR implementations against stuck-on and stuck-open faults [8].

TABLE II summarizes the number of transistors in each majority voter. It is possible to notice that Classical and BAN majority voters have the smallest number of transistors, while the TR Voter presents the highest transistor number.

TABLE II NUMBER OF TRANSISTORS IN EACH MAJORITY VOTER IMPLEMENTATION

Name	Number of transistors
Classical	14
NAND	18
NOR	18
MUX	22
KSHIRSAGAR	30
BAN	14
TR	36



(a) BAN (b) CLASSICAL (c) NAND (d) NOR (e) TR (f) KSHIRSAGAR (g) MUX

Figure 1: Majority Voters under Study

III. METHODOLOGY

This work evaluates delay and power characteristics of the seven majority voters architectures presented previously, considering the aspects of voltage variability. For this analysis, it is also considered the minimum circuits, where the size of NMOS transistors is set as the minimum of the technology and PMOS sizing is considered twice the minimum. The circuits are designed at predictive 32nm High Performance technology [9] and the evaluation is done at electric level, with the NGSPICE electrical simulator [10].

The structure presented in Figure 2 is used in the simulations for performance and robustness evaluation of the voters. The input buffers become the input signals closer to real ones and the output inverters represents the load capacitance. Assuming that a voter is a part of a system, it is important to consider the effect of other devices, and these inverters are a good generalization of the whole system.

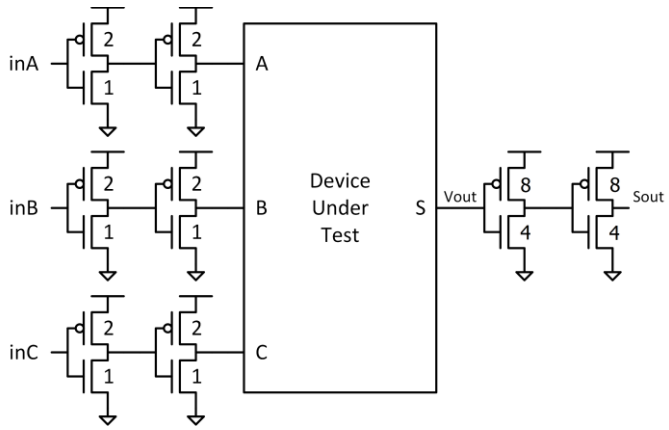


Figure 2 Circuit used in simulations for performance

A logical validation of all majority voters is performed to verify the correct circuit operation. For all timing arcs in the circuit, it is observed values of minimum, maximum, mean (μ) and standard deviation (σ) of the propagation times. The maximum values in timing arcs are analyzed, as they are important to evaluate how the circuit behavior is in the worst case. Power consumption and performance sensibility is computed. All experiments were held at nominal conditions and also considering the voltage variability.

As normally used by the industry in the design of Standard Cell libraries, the impact of voltage variations considers oscillation on 10% of the nominal value of the power supply (Vdd). Therefore, the values adopted, to realize the simulations using CMOS 32nm technology, are from 0.81V to 0.99V with a 30mV step.

IV. RESULTS

First, this work presents the results of power, delay and PDP for the majority voters architectures at nominal conditions without consider variability effects. The second part of the results presents the voltage variability evaluation.

A. Nominal Results

TABLE III presents the nominal results obtained to all the 7 majority voters architectures considering the minimum sizing. Results are divided in maximum, minimum, mean and standard deviation values of propagation time, the total power dissipated in the entire transient simulation, and the power delay product that better represents the energy consumption.

The NAND voter has the lowest maximum value of propagation time and good results for mean and standard deviation. Otherwise, KSHIRSAGAR has the highest maximum value and standard deviation, and also a high average propagation time. BAN voter has the best mean result and minimum value. The TR voter has the highest average propagation time, and the best result for standard deviation.

The power results consider the energy consumption from the supply source of the majority voter and the pass transistor consumption, which is analyzed from the second level of the input's inverters. Considering the best and worst results of power consumption, as shown in TABLE III, NOR voter shows up to 48% of power reduction compared to KSHIRSAGAR voter. The voters NOR and NAND presented similar values of energy consumption. PDP results strengthen the power and timing results, showing NAND as good option when compared to CLASSICAL voter. NAND and NOR presented similar behavior. KSHIRSAGAR and MUX showed up the worst cases.

TABLE III RESULTS OF THE 7 MAJORITY VOTER WITHOUT VARIABILITY EFFECTS, CONSIDERING MINIMUM SIZING

Majority Voter	**Propagation Time (ps)**				**Power (μW)**	**PdP (aJ)**
	Maximum	Minimum	Mean	Standard Deviation		
CLASSICAL	36.01	21.41	29.85	4.85	1.32	47.58
NAND	34.78	19.35	26.87	6.69	1.24	43.06
NOR	36.76	18.12	26.75	6.72	1.20	44.14
BAN	37.20	10.10	22.07	11.88	1.38	51.48
KSHIRSAGAR	61.17	10.98	32.65	22.21	2.30	140.96
MUX	45.55	19.40	31.69	11.12	1.74	79.31
TR	39.13	29.54	34.86	2.86	1.69	65.98

B. *Voltage Variability Results*

The voltage variability affects directly the circuit performance. It is observed in TABLE IV that the majority voter power consumption increases when increasing the voltage. When the voltage is reduced 10% of the nominal value of the power supply, there is around 20% of power reduction for all the majority voters. Analysing PDP values, there is around 3% reduction, except for the NAND voter that reduces 5% and the CLASSICAL voter that shows a different behaviour increasing 0.5% of PDP.

When the power supply nominal value is increased by 10%, the power consumption increases around 24%. Observing the PDP values, there is around 6% increase with the voltage variation, except for the CLASSICAL voter, which presents 9% increase.

TABLE IV POWER RESULTS UNDER VOLTAGE VARIATION WITH MINIMUM SIZING

Majority Voter	Power (µW)						
	0.81V	**0.84V**	**0.87V**	**0.9V**	**0.93V**	**0.96V**	**0.99V**
CLASSICAL	1.05	1.14	1.23	1.32	1.42	1.52	1.63
NAND	0.99	1.07	1.15	1.24	1.33	1.42	1.52
NOR	0.96	1.04	1.12	1.20	1.29	1.38	1.48
BAN	1.10	1.19	1.29	1.38	1.49	1.60	1.72
KSHIRSAGAR	1.83	1.98	2.14	2.30	2.48	2.68	2.88
MUX	1.39	1.50	1.62	1.74	1.87	2.01	2.16
TR	1.35	1.45	1.57	1.69	1.81	1.94	2.07

The Power-Delay-Product (PDP) results under voltage variability are presented in Fig.3. It is possible to observe a similar behaviour between the voters NOR and NAND. The KSHIRSAGAR, MUX and NAND circuits are most sensible to voltage variability, while CLASSICAL voter shows small dependence of the voltage variations.

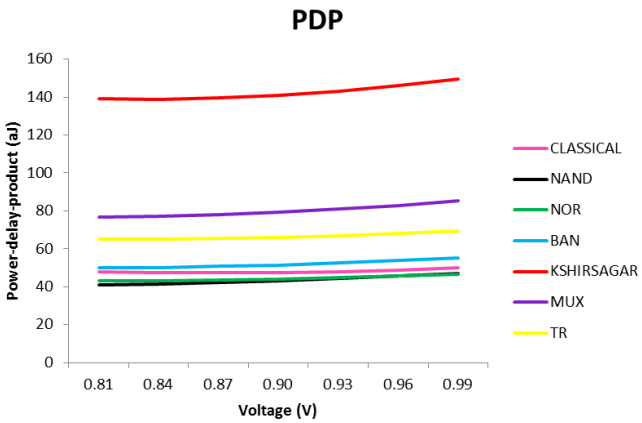


Figure 3 Voltage impact on the majority voter

V. FINAL REMARKS

This work presents the electrical characteristics of majority voters operating under nominal conditions. Also, a voltage variability analysis is performed. Propagation time, power consumption and power-delay-product are explored presenting maximum, minimum, mean and standard deviation values. The results presented in this work are essential to designers explore the best characteristics of each structure.

Observing delay, power and PDP results without variability effects is possible to notice that the BAN voter presents the smallest delay results, producing the smaller delay average. The NOR voter presents the best power consumption between all voters analyzed. The NAND voter presents the best PDP values.

When considering the voltage variability effects, the BAN voter continues to present the best delay results. However, the NAND voter presents lower power consumption and the CLASSICAL voter the best PDP results. Therefore, it is possible to observe that the KSHIRSAGAR voter is the most sensible to voltage variability and the CLASSICAL voter shows small dependence of the voltage variations.

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