Study of Irradiated MOSFET Devices at different Temperature Conditions

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1. Abstract

Radiation disturbs and modifies electrical parameters, as threshold voltage, of electronic devices. Temperature can affect mobility and displacement of carriers on them. The aim of this work is to characterize irradiated MOSFETs and analyze the behavior of thermal annealing processes on different temperatures and conditions, in order to understand the temperature effects in the electrical parameters of irradiated components.

2. Introduction

The increasing miniaturization of electronic components and the greater need for faster and more resistant circuits require that a broader study be performed on the limitations and reliability of the electronic devices, such as MOSFETs, when they are exposed to external interferences [1]. When bias is applied to the gate of a MOSFET, electric charges are attracted to the region between drain and source terminals, creating a channel through which electric current may flow. However, when the device is exposed to ionizing radiation, charges are generated and some of them are trapped as a result of the Total Ionizing Dose (TID) absorbed. Among other effects, these trapped charges promote a variation in the carriers' mobility which has direct effects on the electrical conductivity of the device.

Electric charges generated by TID may be trapped in energy states of the insulating parts of the device [2]. Electron-positron pairs owing to the interaction of radiation with matter generate these trapped charges. This process may occur due to three effects: Compton effect, photoelectric effect and pair generation [1]. The production of electron-positron pairs and its probability of creation by one of these effects depend on the energy of the incident radiation. It is also needed a small amount of energy to create these pairs (e.g. 18 eV per pair in SiO_2) in order to promote an electron from the valence band to the conduction band leaving a positively charged hole behind. The mobility of a conduction band electron is usually much greater than the mobility of a hole [3]. Hence, holes may become trapped in the device oxides for a long time while electrons escape from the oxides in a relatively short time.

Trapped charges in the oxide and at the interface between oxide and silicon affect the device operation, modifying the threshold voltage and the I_{ON}/I_{OFF} ratio of the irradiated device. Device parametric degradation generates uncertainty about its operation.

Techniques such as thermal annealing treatment are used to minimize these effects and to recover electronic devices [4]. This technique involves heating up the device to a temperature sufficiently high and for a time period long enough to promote the rearrangement of earlier trapped charges. Therefore, if a trapped hole receives enough energy, it may escape from the oxide. This energy may come as thermal energy provided by a heat bath [5]. Conversely, if the device is maintained at a temperature that is too low, it is expected that the holes remain trapped for a long time, at least in absence of other energy sources.

Thermal annealing results in the recovery of device initial electrical conditions as a consequence of a recombination of carriers. Standards issued by the European Space Agency (ESA) or by the US Department of Defense regulate the testing of a device [6].

This work shows the behavior and analyzes the parametric recovery of irradiated n-MOSFETs in the CD4007 IC after different thermal annealing treatments. Due to recent researches have reported that this circuit is great responses as a radiation detector, and therefore the transistors showed high sensitivity to the mechanisms of accumulation of charges by radiation dose, this study used the n-type transistor of this IC [7]. The irradiation procedure was performed by a 10-keV X-ray beam [8]. After irradiated, the device was subjected to temperatures between 243 K and 323 K and it was characterized for each increase of 5 K.

3. Experiment

CD4007 is an inverter with two CMOS pairs and a NOT logic gate, which is composed by 3 n-MOS and 3 p-MOS transistors. Although the device is an inverter, this experiment only analyze the behavior of a single MOSFET device, due to its high sensitivity to the effects of TID [7]. In order to evaluate the behavior of the irradiated MOSFETs during thermal annealing, the device was tested on different temperatures and conditions. X-ray irradiation procedure was performed

with a Shimadzu XRD-7000 Diffractometer, shown in Fig. 1, with a 737.4 rad/s dose rate, accumulating TID of 750 krad. A 20-kVvoltage was applied to the X-ray tube terminals, generating a 10-keV effective energy X-ray beam. The epoxy layer of the integrated circuit was removed to eliminate a barrier between the device and the radiation source. It is noteworthy that in the present study was to investigate the behavior of just one of the n-MOSFET.

***Fig. 1** - Detail of the XRD-7000 Diffractometer at Centro Universitário FEI showing the CI placed perpendicular to the X-ray beam*

In order to understand the physical process of trapping charges and the energy states occupied by them, the CI was submitted to an automatic temperature control system, which allowed analyzing the characteristic curve of the device under test (DUT). During electrical characterization, the device was in termal contact with a large metal surface (sample holder), inside a vacuum chamber, as it is shown on Fig. 2. The threshold voltage was obtained through the second derivation of $I_{DS}xV_{GS}$ for a voltage between source and drain of V_{DS} = 100 mV. The Different temperatures were obtained with a system composed by an ARS-2HW closed cycle cryocooler, equipped with a Lakeshore temperature controller. Electrical characterization of the transistors was performed with a NI PXIe-1062Q measurement equipment.

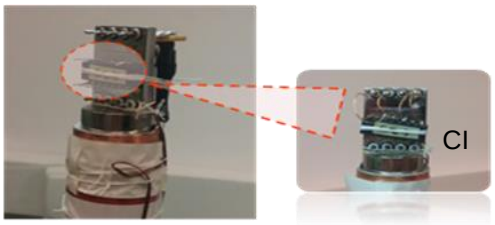

***Fig. 2** - Detail of the CD4007 Integrated Circuit positioned on the cryocooler ARS-2HW sample holder.*

In order to understand the effects of temperature on the physical mechanisms that would trap the charges in the device, two different experiments were conducted:

I – Temperature Ramp Annealing (TRA): in the first experiment, the previously irradiated, unbiased device was subjected to a ramp of increasing temperature that last 2 hours and 20 minutes. Temperature was changed from 243 K up to 323 K, and the device was electrically characterized each 5 K of temperature increase. Source-drain voltage was V_{DS} = 100 mV and temperature was constant during characterization. It is important to emphasize that more than one characteristic curve was obtained at each step of temperature, ensuring that the parameters for n-type device was extracted considering system stability.

II – Steady Temperature Annealing (STA): in the second procedure, the integrated circuit was maintained at a constant temperature of 323 K. In order to check the action of the electric field applied after the system acquire stability in this temperature, one of the devices n-type was unbiased and the other was biased (V_{GS} = 5.0 V) during the thermal treatment. During characterization, source-drain voltage was V_{DS} = 100 mV.

4. Results

4.1. Results for experiment I

For the first experiment (TRA), Fig. 3 presents the threshold voltages for an n-MOS transistor as a function of time of the system, with a variation of 5 K between each step. Fig. 4 presents threshold voltage shifts as a function of temperature for the same experiment.

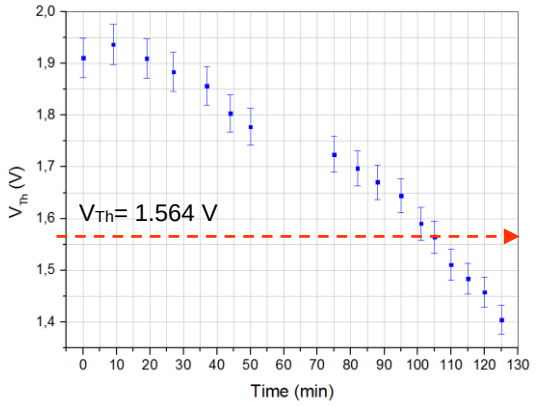

***Fig. 3** – Threshold Voltage on n-MOS transistor with a 750 krad accumulated dose and with temperature ranging from 243 up to 323 K, during more than 2 hours. Red dashed line indicates the threshold voltage after irradiation with stability in room temperature.*

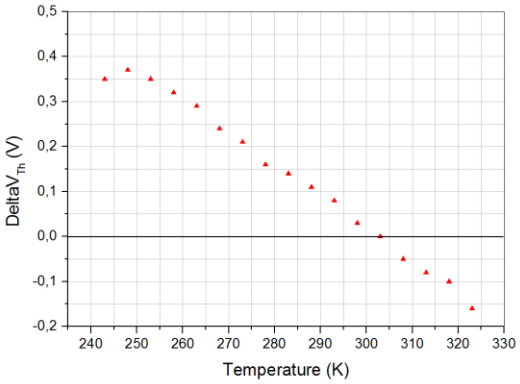

Fig.4 *– Variation of Threshold Voltage (comparison with the initial threshold voltage of V_{Th}=1,56V) versus Temperature curve.*

We can clearly observe that during the first experiment, the threshold voltage decreased with the increasing temperature. When the device is at thermal annealing with a temperature of 243 K its threshold voltage is V_{Th}= (1.910 ±0.038) V, a variation of 0.346 V with its threshold voltage after irradiation and at room temperature of V_{Th}= (1.564 ±0.031) V. On the other hand, its operation voltage at the temperature of 323 K reaches V_{Th}= (1.404 ±0.028) V, which represents a variation of -0.160 V in respect to its initial parameter. Due to the low initial temperatures, trapped holes in the oxide-silicon interface remained trapped. As we increase temperature, some of these initially trapped holes began to free themselves from their traps, affecting the threshold voltage.

Maximum transconductance, which is related with the carriers' mobility [8], as function of increasing temperature is presented in Fig 5. It is possible to observe a decrease of the maximum transconductance with increasing temperature, a consequence of the reduction of the carriers' mobility. We interpret this finding as suggesting that the holes released from interface traps recombine with conduction band electrons in silicon, reducing the carriers' effective mobility.

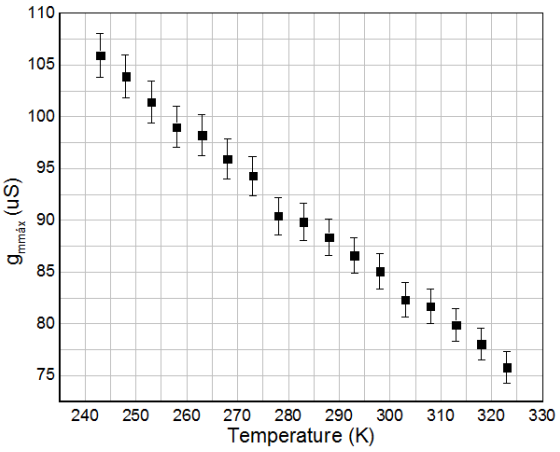

Fig.5 *– Maximum Transconductance ($g_{mmáx}$) versus Temperature for a V_{DS}=100 mV.*

Fig 6 presents the I_{ON}/I_{OFF} ratio as a function of increasing temperature. A large I_{ON}/I_{OFF} ratio is essential for an easy identification of high and low logic states. I_{ON} parameter was taken by extrapolating linear region of log(I_{DS})xV_{GS} curve [9]. On the other hand, I_{OFF} parameter is the current of the device when its voltage between source and gate is 0 V. At a temperature of 243 K the MOSFET has an I_{ON}/I_{OFF} ratio of (344 ±17). This parameter presented some fluctuations during the steps of thermal treatment indicating an increase with temperature. When it is exposed to a temperature of 323 K the ratio reaches (515 ±26). While I_{OFF} had a variation of (9.84 ±2.9) I_{ON} increased from 3.31 ± 4.98 up to 6.26 ± 4.98. This happened because silicon conductivity increases with increasing temperature due to increased carrier density.

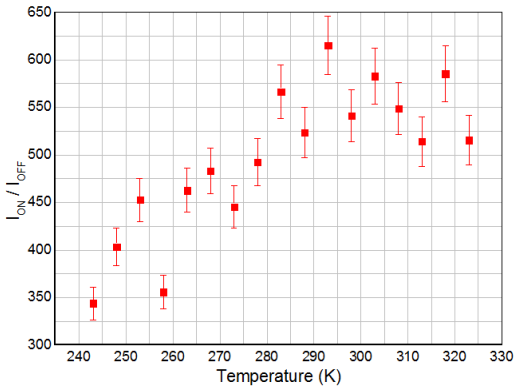

Fig.6 *- I_{ON}/I_{OFF} ratio versus Temperature curve for a n-MOS transistor.*

4.2. Results for experiment II

For the second experiment (STA), the resulting threshold voltage versus time curves, for an unbiased and for a biased n-MOS transistors at T = 323 K are

presented in Fig. 7 and in Fig. 8, respectively. For each condition, the stabilization of the system to determine the action of the bias was reached.

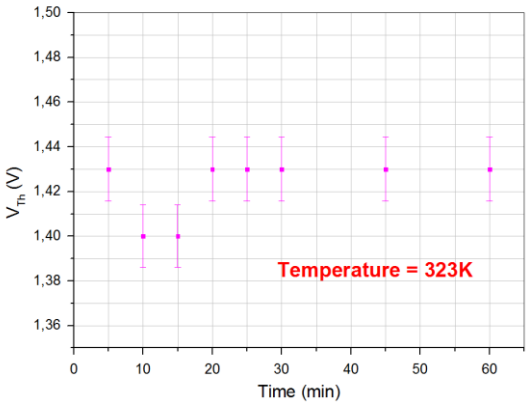

Fig. 7 *– Threshold Voltage versus Time for the unbiased device at temperature of 323 K.*

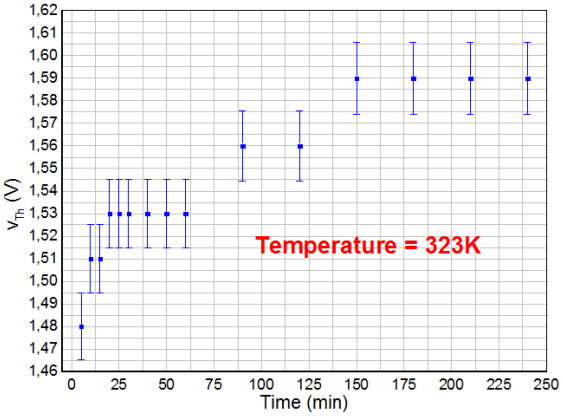

Fig. 8 *– Threshold Voltage versus Time for a constant bias of V_{GS}=5 V with T=323 K.*

In this experiment, it should be noticed that the threshold voltage of the unbiased device does not change even after sixty minutes under 323 K temperature, confirming the stable equilibrium of the system. However, when a biased device under V_{GS} = 5.0 V is subjected to this same temperature, the same system that was stable before, reaches a new level of stability due to the action of the electric field. The threshold voltage increases over time as $V_{Th}(t) = V_{\infty}(1\text{-}A\ e^{-t/\tau})$ with $\tau \approx 90$ min, reaching a V_{Th} = (1.59 ±0.015) V. Hence, we may observe that, in this experimental conditions, it takes some time until the device achieves its final threshold voltage.

5. Conclusions

Temperature dependence of the electrical behavior of n-MOS transistors subjected to radiation was investigated using two experimental settings. In the first experiment, temperature was increased from 243 K up to 323 K. The observed threshold voltage and maximum transconductance shifts were consistent with hole detrapping from oxide-silicon interfacial traps.

In the second experiment, unbiased and biased (V_{GS} = 5.0 V) n-MOS irradiated transistors were maintained at a constant temperature (T = 323 K). Electrical characterization of the devices during thermal treatment showed that there was a significant variation in threshold voltage for the biased device. In fact, we observe that the threshold voltage approached exponentially its steady-state value with a time constant $\tau \approx 90$ min. No significant variation of the threshold voltage was observed for the unbiased transistor during thermal treatment.

New experiments are being performed to verify the correlation between the energy levels of trapped charges by the irradiation process and the charges trapped intrinsically by the device manufacturing process.

6. Acknowledgents

Thanks to Vagner B. Barbeta, Centro Universitário FEI and Projeto CITAR for their support in the experiment.

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