Experimental study of underlap UTBB SOI transistors down to 50 nm channel length

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***Abstract* — This paper presents an analysis of the channel length influence on Ultra Thin Body and Buried Oxide (UTBB) SOl nMOSFET devices based on experimental data. An analysis of the underlap influence on devices with a shorter channel length will be presented based on the front threshold voltage (V_{TF}) and subthreshold swing (SS). The reverse short channel effect (SCE) and the ground plane (GP) influence will also be analyzed.**

Keywords— SOI; Ultra Thin Body and Buried Oxide; Short channel effects; Ground Plane.

I. Introduction

The Silicon-on-Insulator (SOI) technology has been enabling the downscaling of MOSFETs, and more recently, the SOI Ultra-Thin Body and Buried Oxide (UTBB). The UTBB device is a planar technology solution that presents good performance characteristics like high speed, low power and better control of Short Channel Effect (SCE) [1-5]. However, the strong coupling between front and back interfaces for thinner silicon film and buried oxide increases the effect of the substrate potential drop on the devices parameters.

In order to minimize the substrate effect a Ground Plane (GP) implantation under the buried oxide is usually used. The study and modeling of the influence of GP have been reported in [6-9].

Devices that have the non-self-aligned gate with the drain and source (underlap or extensionless) has an effective channel length modulated by the gate applied bias, which controls the currents at the channel and the Short Channel Effect (SCE). [10].

This paper presents an analysis of the Short Channel Effect (SCE) on UTBB devices with six different channel length (965, 215, 115, 95, 70 and 50 nm) with and without Ground Plane implantation. The SCE analysis was performed based on two basic parameters: threshold voltage (V_{TF}) and subthreshold swing (SS).

There was also a comparison of the front threshold voltage (V_{TF}) as a function of back gate bias (V_{GB}) between the experimental data and the model [11] for devices with and without ground plane implantation.

II. Experimental Details

The studied UTBB SOI nMOSFET devices were fabricated at imec, Belgium, in an SOI substrate with a final silicon film thickness (t_{Si}) of 6nm and a buried oxide thickness (t_{oxb}) of 18 nm.

The gate stack is composed of 5nm SiO_2 thermal oxide and a TiN metal gate electrode. These devices were fabricated for 1T-DRAM applications, where the gate oxide thickness (t_{oxf}) is thicker to obtain a small gate current [12-13].

The silicon film has the natural doping concentration (Na - around 10^{15} cm^{-3}), i.e., there is no intentional extra channel doping implantation, the substrate concentration (Na_{SUB}) is also around 10^{15} cm^{-3}. There are devices that have a Ground Plane implantation under the buried oxide, by a boron implantation at 25keV and $5x10^{13}$ cm^{-2}. The analyzed channel lengths were L= 965, 215, 115, 95, 70 and 50 nm, with a constant channel width W=1μm and an underlap of 10 nm. More process information can be found in [13].

A schematic cross-section of the UTBB SOI nMOSFET is shown in Figure 1, where V_S, V_D, V_{GF} and V_{GB} is the source, drain, front-gate and substrate (or back-gate) voltage, respectively.

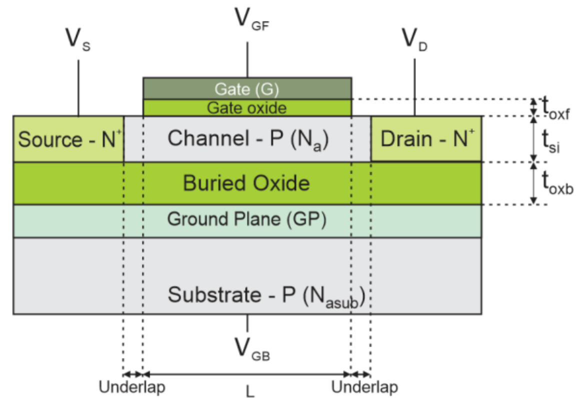

Fig. 1. A schematic cross-section of an UTBB SOI device with GP and Underlap.

The measurements were done with an Agilent B1500 system. The drain current (I_{DS}) curve as a function of front gate bias (V_{GF}), with a drain voltage (V_{DS}) equal to 50 mV were

measured with three different values of back gate bias in the triode region, V_{GB} = -2V, 0V and 2V.

The extraction of front threshold voltage (V_{TF}) was made based on the second derivative method, which is applied on I_{DS} as a function of V_{GF} curve [14].

III. Results and Discussion

The experimental drain current (I_{DS}) as a function of front gate bias (V_{GF}) for devices with V_{GB} = 0V and without GP and with GP is presented in figures 2 and 3, respectively.

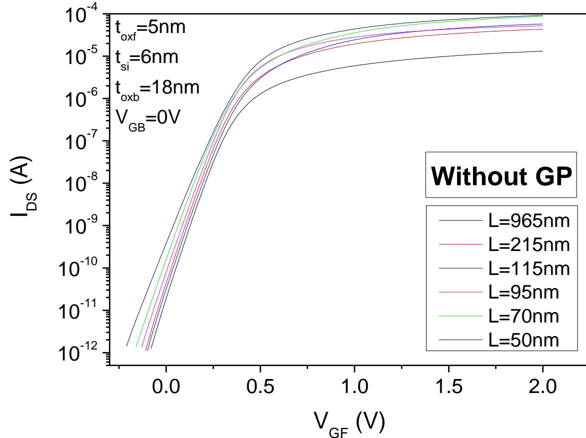

Fig 2. Drain current as a function of front gate bias, with back gate bias equal to 0V and without GP.

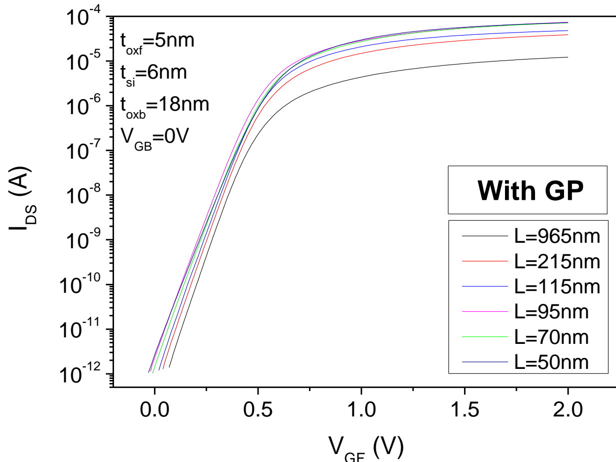

Fig 3. Drain current as a function of front gate bias, with back gate bias equal to 0V and with GP.

As known from the theory [15], the current level grows while the channel length is reduced, and it is observed on figures 2 and 3. Besides this, there is a I_{DS} shift to a smaller front gate bias as the channel length is reduced until L=95nm. For shorter devices, a rebound of I_{DS} was observed and these values are shown in figure 4.

Figure 4 shows the front threshold voltage (V_{TF}) as a function of the channel length (L). As mentioned before a rebound of V_{TF} values occurs for very short devices due to the reverse Short Channel Effect (SCE). It means that the underlapped regions inversion is dependent on the fringing field and due to the spacer be thicker than the gate oxide, a higher front gate voltage is needed. For channel length smaller than 95nm, the influence of the front threshold voltage of the underlap part becomes more important, affecting the effective V_{TF} of the device. It is observed for both devices with and without GP implantation.

The threshold voltage for devices with GP implantation is higher than those without one due to the smaller surface potential at the third interface.

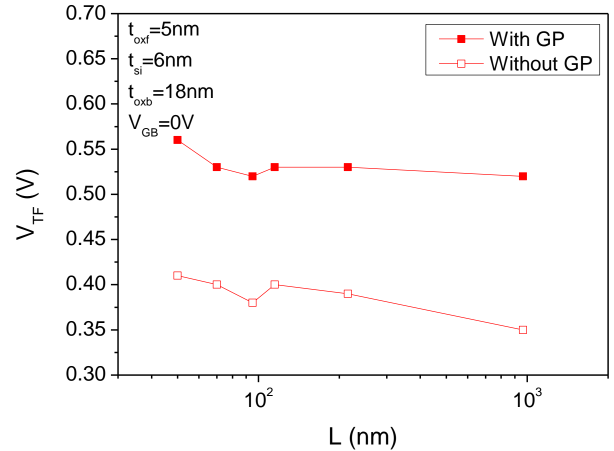

Fig 4. Experimental curve of front gate bias as a function of the channel length with back gate bias equal to 0V.

Figure 5 presents an experimental curve of subthreshold swing (SS) as a function of channel length (L). Comparing the SS values for devices with and without GP a negligible variation was observed. The maximum variation between them occurs for L=115nm (ΔSS=4.27mV/dec). This behavior can be explained by the fact that the buried oxide capacitance predominates in both devices. For L smaller than 95nm an increase of SS values were obtained showing the usual SCE for both devices (with and without GP).

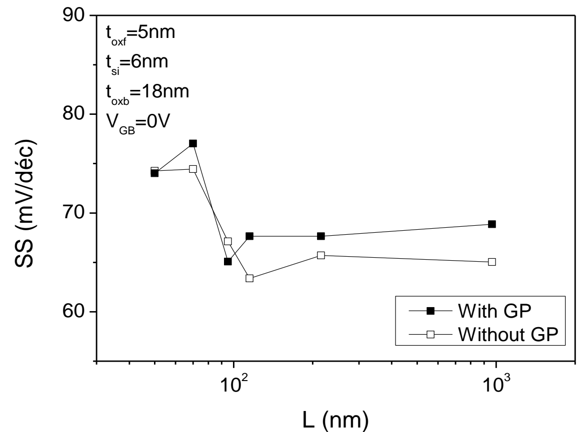

Fig 5. Experimental curve of subthreshold swing as a function of the channel length with the back gate bias equal to 0V.

Figure 6 shows a comparison of the experimental values of front threshold voltage for V_{GB}=-2, 0 and 2V with the model for the largest channel length (L=965nm), where there isn't the presence of SCE (for devices with and without GP).

It is observed a very good fit between the experimental data and the model [11] for all V_{GB} values.

The analytical model presents the third interface behavior with a potential applied at the substrate and its influence on the V_{TF} value. When the second interface is depleted, the third interface can be accumulated, depleted or inverted. When V_{GB} is about 2V the third interface is accumulated and the V_{TF} tends to increase, until V_{GB} about 0V when the third interface is depleted and in this region V_{TF} tends to be constant, then applying a negative potential at the substrate, the third interface tends to invert and the V_{TF} increases with the potential. This model was studied by Itocazu et al [9].

Figure 7 shows a comparison of the experimental V_{TF} values for V_{GB}=-2, 0 and 2V with the model for the shorter channel length (L=50nm) for devices with and without GP. It is observed when V_{GB}=0V, there is a reverse SCE occurring that can be explained by the underlap region influence on V_{TF} as explained before. The experimental values are slightly higher than the model curve, because this model does not consider the underlap region and the channel length.

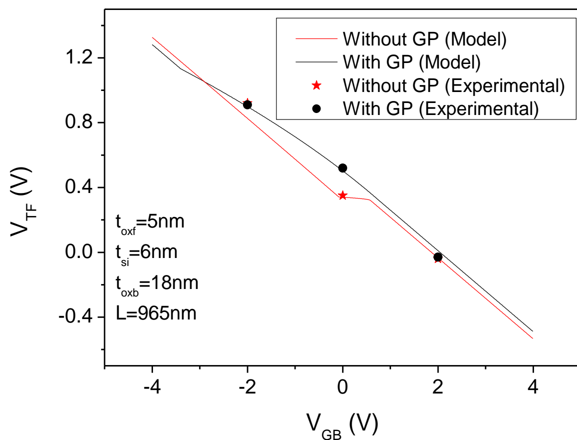

Fig 6. Comparison between the model and the experimental data curve of the threshold voltage as a function of back gate bias for L=965nm.

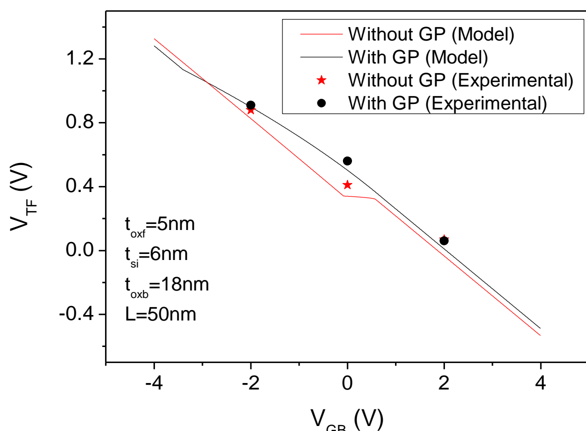

Fig 7. Comparison between the model and the experimental data curve of the threshold voltage as a function of back gate bias for L=50nm.

IV. Conclusion

In this paper the analysis of the channel length on Ultra Thin Body and Buried Oxide (UTBB) SOI nMOSFETs was investigated based on experimental data.

It was verified that for devices with channel length shorter than 95 nm occurs the reverse SCE on V_{TF} roll-off that was explained by the underlapped regions that interfere on the bias to invert the channel, it means that the front threshold voltage increases while the channel length is reduced.

The curve of subthreshold swing presented the classical SCE, when the channel length is reduced the SS increases. No significant influence of GP was observed in SS parameter.

When comparing the experimental results with the model for threshold voltage, with and without a ground plane implantation, a good fit was obtained.

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