Influence of Substrate Bias in Electric Parameters of Multiple Gate SOI Transistors with Thin Buried Oxide Layer

Érika Harumi Yamanaka, Rodrigo Trevisoli Doria
Centro Universitário da FEI: Electrical Enigeering Department – São Bernardo do Campo, Brazil
e-mail: erikaharumi1@hotmail.com

***Abstract*—This work deals with the multi-gate SOI MOSFET transistor device and has the purpose of analyzing its performance when the UTBB (Ultra Thin Body and Buried Oxide) technology is associated with the variation of substrate bias (V_{BS}). The behavior of the main digital and analog electric parameters have been evaluated through numerical simulations for devices with different fin heights and buried oxide thicknesses (H_{fin} and t_{box}, respectively). It has been observed that the dependence of the electric parameter on substrate bias is higher for smaller H_{fin} and t_{box} and the intrinsic voltage gain for such devices can be better than the others for negative V_{BS}.**

Keywords—Multi-gate; Substrate Bias, UTBB, Electrical Parameters

INTRODUCTION

The Silicon-On-Insulator Metal-Oxide-Semiconductor Field Effect Transistor (SOI MOSFET) consists on a MOS device whose active silicon layer is separated from the substrate by an insulator layer called buried oxide (BOX). The presence of the BOX layer results in a higher processing speed, reduction of parasitic capacitances, lower short channel effects (SCEs) and provides greater longevity to the devices [1]. These advantages, especially the reduced SCEs, are extremely important for the continuous downscaling of the devices dimensions required by the microelectronics industry. As the devices dimensions are reduced, the amount of channel charges controlled by the source/drain depletion regions becomes important with respect to the total charge controlled by the gate. The poorer gate control on the channel results in several SCEs, such as the decrease of the threshold voltage (V_{TH}) with the channel length (L) reduction. The BOX presence enhances the capacitive coupling of fully depleted structures, reducing SCEs.

Aiming at even higher density integration and better gate control on the channel region to reduce even more the short channel effects, extending the Moore's law [2] different multiple gate transistors have been proposed. Multiple gate devices can be fabricated on SOI substrates [3] and usually present a gate stack that covers more than one face of the active silicon layer as evidenced in Fig. 1, which presents the 3D scheme of a tri-gate SOI transistor. In tri-gate transistors, there are conducting channels on the three sides of the vertical fin (on top and both sidewalls).

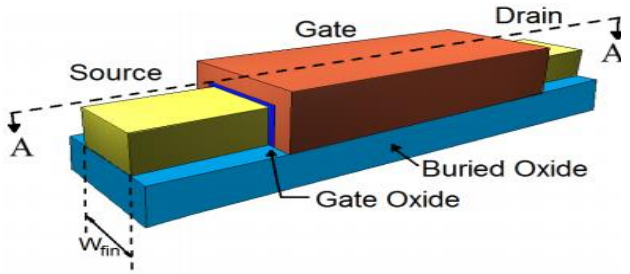

Fig. 1. Transistor SOI FinFET of tri-gate representation.

Recently, in order to improve the electric performance of SOI transistors, a new technology, so-called UTBB (Ultra Thin Body and Buried Oxide) has been incorporated to planar SOI fully depleted devices [4]. Such technology proposes the fabrication of SOI devices with extremely thin silicon and buried oxide layers. The reduction of the silicon layer thickness (H_{fin}) down to ~10 nm [5] can improve significantly the capacitive coupling, reducing SCEs whereas the thin BOX layer (around 20 nm) allows for using the substrate as a back gate not short-circuited with the top one [6]. The UTBB fabrication process proposed by STMicroelectronics [7] allows for accessing the substrate bias (V_{BS}) of individual transistors in a circuit, making it possible the use of different back bias in different devices with the purpose of enhancing the overall performance of the circuit.

Several papers have shown that the substrate bias of planar transistors can be adjusted to improve the device performance according to the application. Positive back gate bias can lead to a reduction on the threshold voltage, making switching faster whereas negative V_{BS} increases V_{TH} resulting in lower leakage at off-state [8].Similarly, negative V_{BS} has shown to improve the analog performance of the devices [9].That technology has been applied mainly in single gate SOI devices. However, there are no major technological obstacles to manufacture UTBB of multiple gates. Therefore, this work has as main objective to verify the behavior of the electrical parameters of multiple gate SOI transistor with thin buried oxide layer when the substrate bias is varied.

DEVICES CHARACTERISTICS

The study of the V_{BS} effect on the performance of tri-gate transistor was performed through 3D numerical simulations performed in Sentaurus Device TCAD [10]. Along the simulations, the devices were defined with silicon height (H_{fin}) of 20 nm and 60 nm, silicon width (W_{fin}) of 20 nm, channel doping concentration of1×10^{15} cm^{-3} and buried oxide thickness(t_{box}) of 20 nm and 150nm.The studied devices present effective oxide thickness (EOT) of 2 nm. The channel length

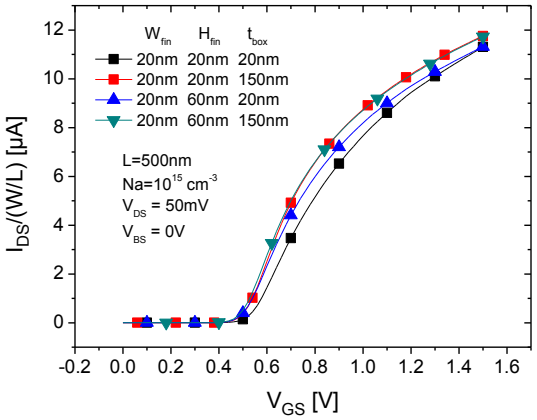

Fig. 2. (A) Normalized drain current as a function of the gate voltage for a substrate bias of 0 V.

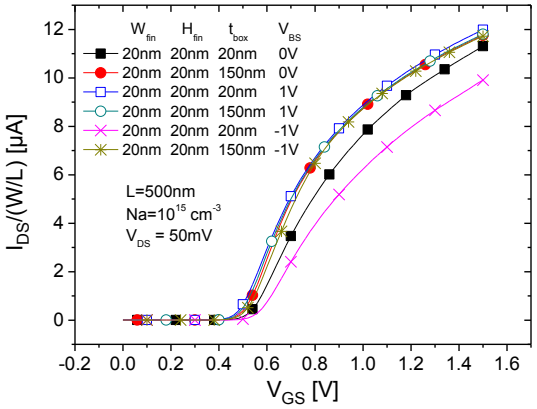

Fig. 2. (B) Normalized drain current as a function of the gate voltage for substrate bias varying from -1V to 1V and for two dimensions.

was considered equal to 500 nm to avoid the occurrence of short channel effects. In order to guarantee that the simulation results are in agreement to experimental data, the simulated I-V curves obtained for the transistor with W_{fin} = 20 nm, H_{fin} = 60 nm and L = 500 nm were validated to the ones from [11].

In Fig. 2, it is shown the simulated curves of the normalized drain current ($I_{DS}/(W/L)$, being $W = 2H_{fin}+W_{fin}$) as a function of the gate voltage for a long-channel device with L = 500 nm for different H_{fin} and t_{box} biased at a drain bias of V_{DS} = 50 mV. It is necessary to normalize I_{DS} by the devices dimensions since gate area is different among the structures.

In Fig. 2 (A) the substrate bias was V_{BS} = 0 V and it is noticed a slight difference between the four dimensions mainly due to the different threshold voltage of the devices. Also, the devices with thinner t_{box} present a slight different capacitive coupling than the others, which has modified the drain current variation rate with V_{GS}. In Fig. 2 (B), it is shown the curves of the normalized I_{DS} for transistors with H_{fin} = 20 nm and different t_{box}. The substrate bias has varied from negative to positive and it can be noted that the difference between the curves for different V_{BS} is larger when t_{box} is reduced, demonstrating the better coupling of this structure. For devices with t_{box} = 150 nm, the V_{BS} variation has negligibly affected the curves.

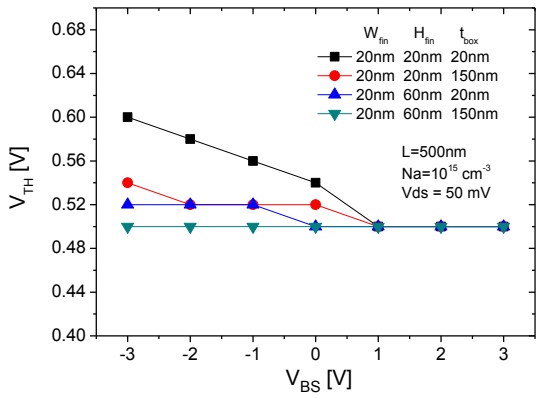

Fig. 3. Threshold voltage as a function of the substrate bias extracted from Fig. 2 for V_{DS} = 50 mV.

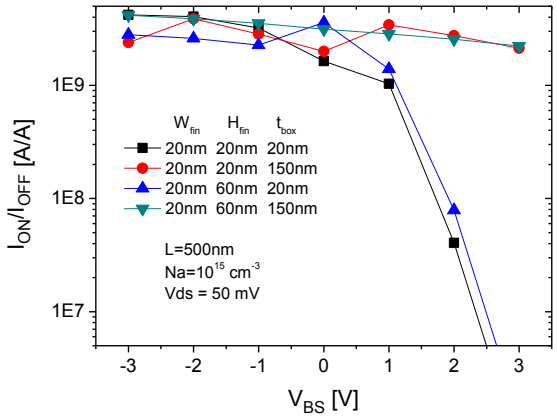

Fig. 4 Ratio of current in on state and current in off state as a function of the substrate bias.

The threshold voltage (V_{TH}) extracted from Fig. 2 is presented in Fig. 3 as a function of the substrate bias for different transistor dimensions. The threshold voltage (V_{TH}) was extracted through the method of the second derivate of the drain current as a function of the gate bias [12]. From this figure, it can be noted that the threshold voltage varies significantly when the substrate bias is changed from 3 V to –3 V in the device with thinner H_{fin} and t_{box} whereas no V_{TH} variation has been obtained for the transistor with thicker H_{fin} and t_{box}. From Fig. 3, it can also be mentioned that the V_{TH} dependence on V_{BS} is not linear in the entire range. For negative V_{BS}, the silicon layer depletion associated to the back bias is reduced mainly in the device with H_{fin} and t_{box} = 20 nm. Thus, the gate bias needs to be increased in order to deplete the entire silicon layer, which increases V_{TH}.

Based on the threshold voltage in the Fig. 3 it is possible to obtain the current in switched on state (I_{ON}) considering I_{ON} = I_{DS} at V_{TH}+ 1 V for devices biased at each substrate voltage. On the other hand, the switched off state (I_{OFF}) was obtained by subtracting 0.5 V from the threshold voltage. The ratio of those currents (I_{ON}/I_{OFF}) is presented in Fig. 4 as a function of the substrate bias.

The I_{ON}/I_{OFF} ratio decrease when the thickness of buried oxide is smaller and the substrate bias is positive and high

because these devices start to present a conduction canal within the buried oxide interface which increases I_{OFF} even for negative V_{GS}.

ANALOGIC OPERATION

The same structures have been used for the evaluation of the analog operation of the devices, but the I_{DS} x V_{GS} curves have been simulated for a drain bias of V_{DS} = 1 V. The substrate bias continues to vary from -3 V to 3 V.

Firstly, in the Fig. 5 (A) it is analyzed the transconductance, (g_m) which was extracted in the saturation region by the drain current derivate as a function of overdrive gate voltage (V_{GT} = V_{GS} – V_{TH}). The g_m curves are presented in Fig. 5 (A) for substrate bias varying from -2 V to 2 V for the transistor with H_{fin} and t_{box} = 20 nm, since this device is more sensitive to the substrate bias variation. The transconductance represents the effectiveness of the drain current control by the gate voltage andone can see that an increase of about 20% is obtained when V_{BS} is varied from -2V up to 2V. This behavior is associated with the beginning of the formation of an inversion region in the interface between the active silicon region and buried oxide.

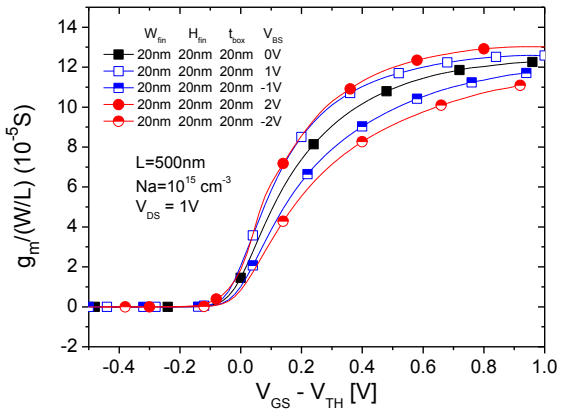

Fig. 5.. (A) Normalized transconductance as a function of overdrive gate voltage for the same dimension and substrate bias varying from -2 V to 2 V.

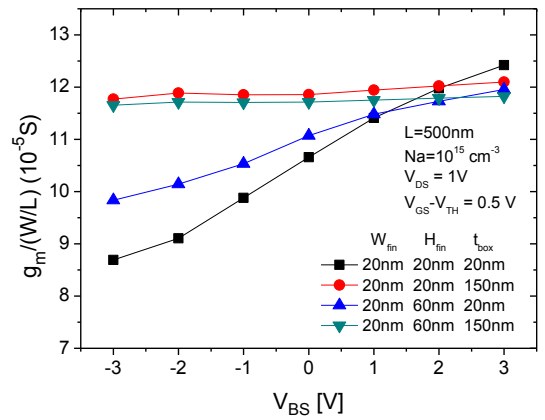

Fig. 5. (B) Normalized transconductance as a function of substrate bias varying from -3 V to 3 V for different dimensions and gate voltage V_{GS} = 1 V.

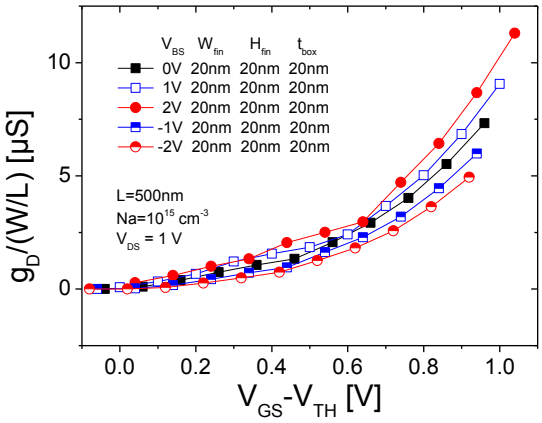

Fig 6. (A) Normalized output conductance as a function of overdrive gate voltage for the same dimension and substrate bias varying from -2 V to 2 V.

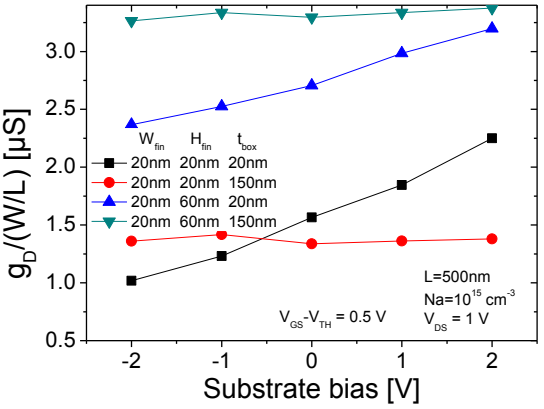

Fig. 6. (B) Normalized output conductance as a function of substrate bias varying from -2 V to 2 V for different dimensions.

This layer enables a larger drain current close to the bottom of the silicon layer, which increases g_m.

In Fig 5 (B) the influences of negative and positive substrate biases in the tranconductance are shown. It can be observed that there is more dependence of g_m for smaller thickness of buried oxide t_{box} = 20nm and the height H_{fin} does not present relevance. As the cutoff frequency is proportional to g_m, when the circuit to be projected requires high cutoff frequency, it can be applied a high substrate bias to the device of smaller dimensions.

Another important parameter for the analog operation of MOS transistors is the output conductance (g_D) which is obtained through the first order derivative of the I_{DS} x V_{DS} curve. In order to evaluate the behavior of g_D against V_{GS} – V_{TH}, it was necessary to simulate a family of I_{DS} x V_{DS} curves for several V_{GS}– V_{TH} from 0 V up to 1 V with steps of 0.1 V for the devices biased at different V_{BS}. In the Fig. 6 (A), the substrate bias influence is noticed in the graphic for the transistor with H_{fin} = t_{box} = 20 nm, which is the device most sensitive to V_{BS} variation. As the gate voltage is incremented, one can observe an increment of g_D for any V_{BS} bias. This behavior is associated to the regime of operation of the devices. For small gate voltages,

the devices are biased deeper in saturation and, as V_{GS} is increased, the devices move to the triode regime, where the dependence of the drain current on V_{DS} gets higher. This effect is more pronounced for large positive V_{BS} since the back interface gets closer to the inversion. In Fig. 6 (B), g_D is presented as a function of the substrate bias in the range from -2 V to 2 V for devices with different dimensions. For both devices with gate oxide thickness of 150nm, g_D has presented the same behavior, being insensitive to V_{BS} variation. The same occurs with the devices with gate oxide thickness of 20nm. In this case, it can be observed a huge increase on g_D when the transistor V_{BS} is varied from -2V up to 2V. When a high substrate bias is applied to the transistor, the interface with buried oxide tends to invert making the operating point closer to the triode region, which degrades the output conductance.

The intrinsic voltage gain (A_V) is obtained from the ratio between transconductance and the output conductance and is presented in Fig. 7 (A) for the transistor with thinner H_{fin} and t_{box} as a function of V_{GS}– V_{TH} for different substrate bias from -2 V to 2 V. As it could be expected, the intrinsic voltage gain reduces with the increase of V_{GS} as the devices approach to the triode regime. Anyway, the largest A_V is obtained for V_{BS} = -2V since the transistor is biased deeper in saturation. In Fig. 7 (B), it is shown the intrinsic gain as a function of substrate bias for transistors with different dimensions. For devices with thicker t_{box}, the gain remained stable for positive and negative substrate bias. The most noticeable curve occurred with the smaller H_{fin} and t_{box} transistor, where the substrate bias had more influence in the intrinsic voltage gain. For V_{BS} = -2V, a slight improvement of was obtained with respect to all the other devices. This occurs due to the extremely lower output conductance presented by this transistor.

CONCLUSIONS

The current paper has presented an analysis on how the influence of the substrate bias affects the performance of triple gate SOI MOSFETs fabricated with thin buried oxide and silicon layers. It has been shown that when both the buried oxide and the silicon layer are reduced together, the application of different substrate biases can modulate the threshold voltage of the transistors similarly to the observed in the UTBB technology. Thus, the adequate back bias can be chosen when either low leakage or faster switching are required. Additionally, it was observed that devices with thin silicon and buried oxide layers can provide larger transconductance than others with different dimensions when a larger V_{BS} is applied whereas a negative back bias results in enhanced output conductance, which directly impacts the intrinsic voltage gain of the devices, leading to a better A_V than the obtained in devices with different dimensions biased at similar conditions.

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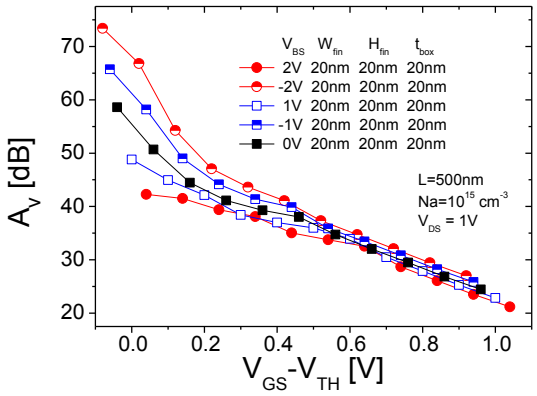

Fig. 7. (A) Gain as a function of gate voltage for the same dimension and substrate bias varying from -2 V to 2 V.

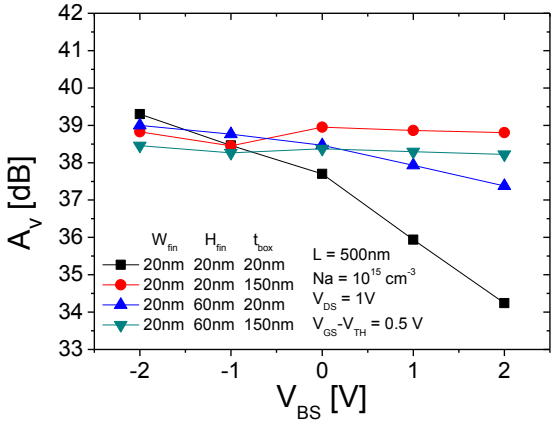

Fig. 7. (B) Gain as a function of substrate bias varying from -2 V to 2 V for different dimensions and gate voltage V_{GS} = 1 V.

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