

Study of Breakdown Voltage in Power MOSFETs in Harsh Environments

N. C. C. Merzbahcer¹, M. Kawano¹, K. Stylianos¹, D. A. Arrabaça¹, M. Rodrigues¹ and M. Galeti¹

¹Centro Universitário da FEI - São Bernardo do Campo, Brasil

e-mail: merzbahcer.cris@hotmail.com

Abstract— This work aims to study the breakdown voltage in power MOSFET transistors in harsh environments. The influence of technological parameters, as doping concentration and carrier lifetime, were studied as well as the high temperature and radiation exposure. The breakdown voltage showed strong dependence with the doping concentration of the drift region. The impact of carrier lifetime variation on the breakdown voltage also was analyzed for this structure and was possible to observe that there is an invariant bias point with the carrier lifetime. The dynamic behavior of the power MOSFET was analyzed after being exposed to radiation, indicating to be further sensitive for lower temperatures and higher drift doping region. All results presented were obtained through Two-dimensional numerical simulations.

Index Terms— Breakdown Voltage, Harsh Environments, Power MOSFETs, Single Event Effect.

I. INTRODUCTION

The significant growth in demand for solutions related to power electronics area has elected the power metal–oxide–semiconductor field effect transistors (MOSFETs) as an alternative in DC-AC converters and in power supplies thanks to their low conduction power loss, high input impedances and high switching speed capabilities [1]. An important feature of power MOSFET devices is their ability to withstand high voltages. In these devices the ability to support high voltages without the onset of significant current flow depends on the electric field distribution within the structure. The power MOSFET design optimization must be performed to meet the breakdown voltage requirements while minimizing the on-state voltage drop to reduce the switching power dissipation. However, the device behavior also depends on the operational environment as temperature variation and radiation exposure. Device failures can occur because of long time of continuous exposure to radiation environment, total dose effects [2] or as a result of radiation transient of high energy particle, single event effects (SEE) [3]. Single Event Upset (SEU) occurs by the penetration of energetic particle within a device. When a particle penetrates a reverse biased junction, a plasma track is produced along the particle path, where electron-hole pairs are generated [4]. When a heavy ion penetrates through a power MOSFET biased in the off state, blocking mode, transient currents are generated and turn on a parasitic BJT inherent to the device structure. Because of a regenerative feedback mechanism, BJT collector currents increases leading breakdowns junction, creating a permanent short between the source and drain and rendering the MOSFET useless [5].

The motivation for this work is to investigate the influence of technological parameters, as doping concentration and carrier

lifetime, in the breakdown voltage behavior when the power MOSFET devices are in Harsh Environments.

II. NUMERICAL SIMULATIONS

A cross-section of the MOSFET structure is illustrated in Fig. 1. Two-dimensional numerical simulations were performed using the Atlas (SILVACO) [6], including models for recombination, photo-generation, impact ionization, narrowing of the energy bands, mobility and lifetime of carriers. The power MOSFET transistors analyzed in this paper were simulated with the parameters presented on Table I.

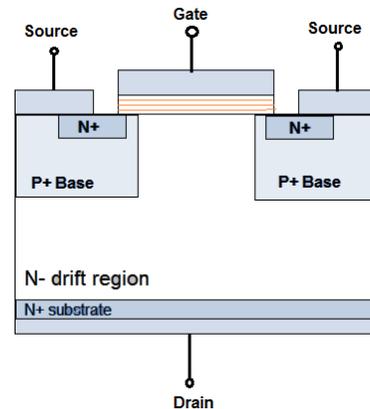


Fig. 1 – Schematic cross-section of a MOS power transistors.

TABLE I
TYPICAL PARAMETERS FOR MOS STRUCTURE USED IN THE SIMULATIONS.

Parameter	Value	Unit
N+ substrate thickness	14,2	μm
N- drift thickness	28	μm
P+base thickness	8	μm
N+ source regions thickness	1	μm
N+ substrate width	25	μm
N- drift width	25	μm
P+base width	8	μm
N+ source width	3,9	μm
N+ substrate doping	1E20	cm^{-3}
N- drift doping	5E15	cm^{-3}
P+base doping	1E17	cm^{-3}
N+ source regions doping	1E20	cm^{-3}
Gate oxide thickness	0,05	μm

The breakdown voltage of a power semiconductor device is one of its most important characteristics. Together with its maximum current, this parameter determines the power rating of the device [7]. Figure 2 shows the Schematic that illustrates the extraction of breakdown voltage from the I-V behavior of

the power MOSFET during the operation in the blocking mode, $V_{GS}=0V$.

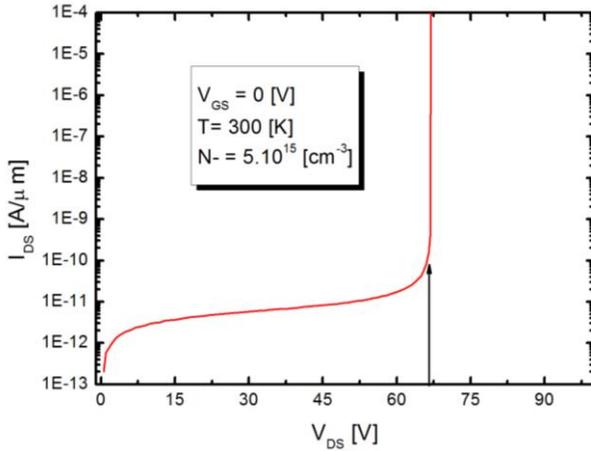


Fig. 2 - Illustration of breakdown voltage extraction.

III. SIMULATIONS RESULTS

A. Technological Parameters

Figure 3 illustrates the drain current as a function of the drain bias at room temperature, with the doping concentration variation of the drift region. A significant reduction in breakdown voltage device was observed with the doping concentration increase in this region. For the lower doping concentration in the drift region, the maximum depletion width in the P-N junction is larger; therefore, it can sustain a much larger electric field.

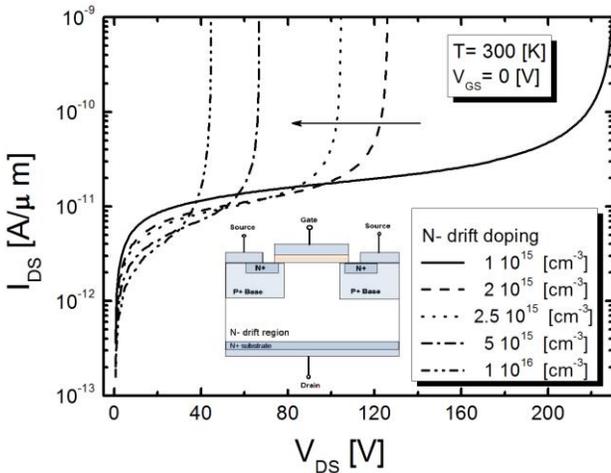


Fig. 3 - I_{DS} as a function of the V_{DS} , with the doping concentration variation.

Figure 4 shows the electric field behaviour as a function of the depth device. The critical electric field is a useful parameter for identifying the onset of breakdown in power MOSFET structures, due to the very strong dependence of the impact ionization with the electric field strength. The breakdown voltage can be usually assumed to occur when the electric field within any local region of a power device approaches the critical electric field [8]. The electric field triangular behavior is particularly true for devices with abrupt junction.

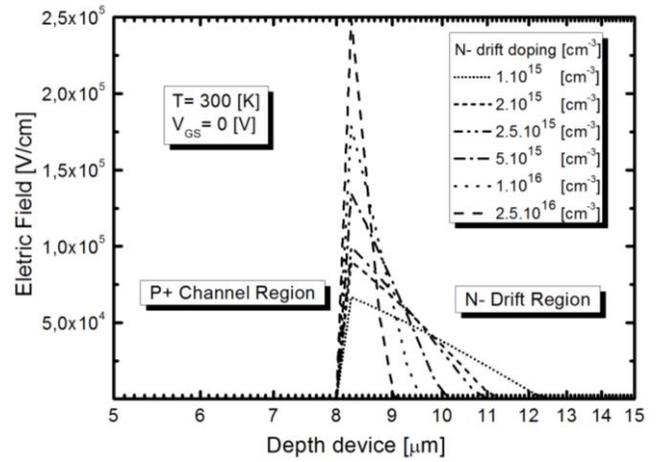


Fig. 4 – Electric field as a function of the depth device.

Figure 5 presents the drain current as a function of the drain bias, for different carrier lifetime, during operation in the blocking mode ($V_{GS}=0V$). The carrier lifetime is often used as a process control parameter due to its strong dependence on the density of crystal defects induced by wafer manufacturing [9]. It is known that the leakage current observed for $V_{GS}=0V$ is proportional to carrier lifetime, Eq. 1. This leakage current is inversely dependent to the carrier lifetime, as a result it is possible to observe that with the increase on the effective carrier lifetime ($(\tau_n + \tau_p)/2$) a reduction on the leakage current level for the same doping concentration. Another important point is related to the reduced breakdown voltage with the increased carrier lifetime. The power MOSFET structure contains a parasitic bipolar transistor formed between the N+ source region, the P-base and the N-drift region [10]. With the increase on the carrier lifetime, it is known that the current gain of the N-P-N bipolar transistor is enhanced. As a result, a reduction in the breakdown voltage is observed for larger carrier lifetime. Due to competition from both phenomena, the reduction of leakage current and the increase of the current gain parasitic bipolar transistor, it is possible observe a drain bias that there is not current variation with carrier lifetime.

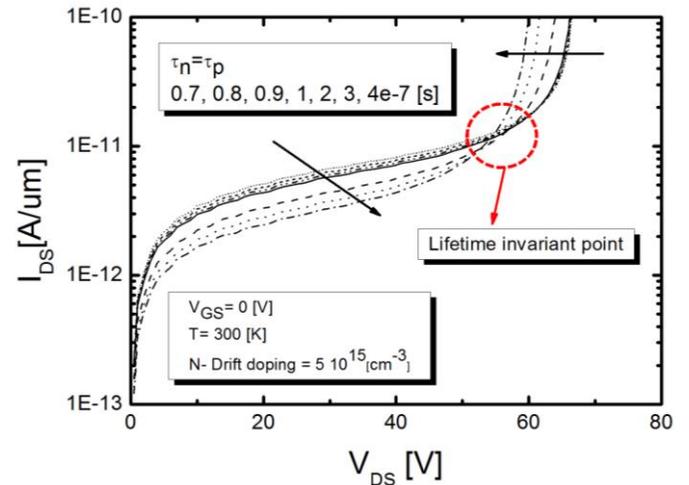


Fig. 5 - I_{DS} versus V_{DS} curves with the variation of the lifetime of the carriers.

B. Temperature

Figure 6 shows the I_{DS} as a function of the V_{DS} , with the temperature variation from 300 to 550K. It can be observed that the drain current during operation in blocking mode ($V_{GS}=0$ V) is strongly influenced by temperature variation due to the dependence of this current with the intrinsic concentration as Eq. 1 [11].

$$I_{leak} = qA \left(\frac{D_n}{\tau_n} \right)^{\frac{1}{2}} \frac{n_i^2}{N_a} + qA \frac{n_i W}{\tau_e} \quad (1)$$

Where q is the electron charge, A is the junction area, D_n is the electron diffusion coefficient, τ_n and τ_p is the electron and hole lifetime, n_i is the intrinsic carrier concentration, N_a is the doping concentration, W is the depletion width of and $\tau_e = (\tau_n + \tau_p) / 2$ is the effective lifetime. Despite the leakage current increase for higher temperatures, the breakdown voltage is increased due to reduction in carrier mobility which decreases the impact ionization near of the drain region.

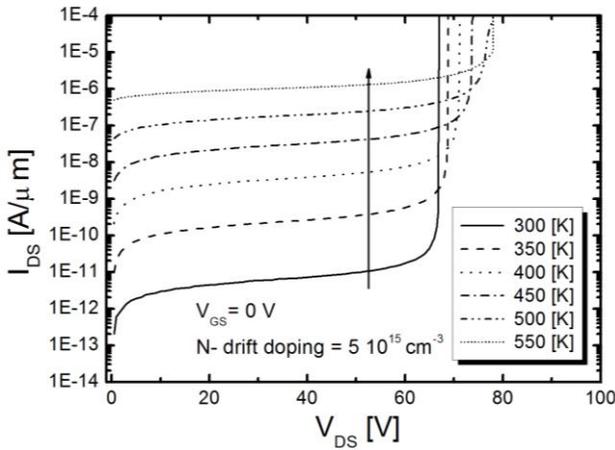


Fig. 6 - I_{DS} as a function V_{DS} curves with the temperature variation.

C. Radiation

The results discussed in this section were based on two-dimensional numerical simulations with exposure to radiation. The beam of particle is emitted in the center of the source regions, the first beam at $3,5 \mu\text{m}$ and the second in $22,5 \mu\text{m}$, as specified in Fig. 7. The main effect caused by the incidence of radiation is the electron-hole pairs generation increase which can be observed through gaps concentration shown in Fig. 7. The simulations were performed with $V_{GS}=0\text{V}$, $V_{DS}=60\text{V}$, $T=300\text{K}$, $N\text{-drift doping}=5.10^{15} \text{ cm}^{-3}$ and $b.\text{density}=0,02 \text{ pC}/\mu\text{m}$. So for instance, a $b.\text{density}$ value of $0,02 \text{ pC}/\mu\text{m}$ is equivalent to $2 \text{ MeV}\cdot\text{cm}^2/\text{mg}$.

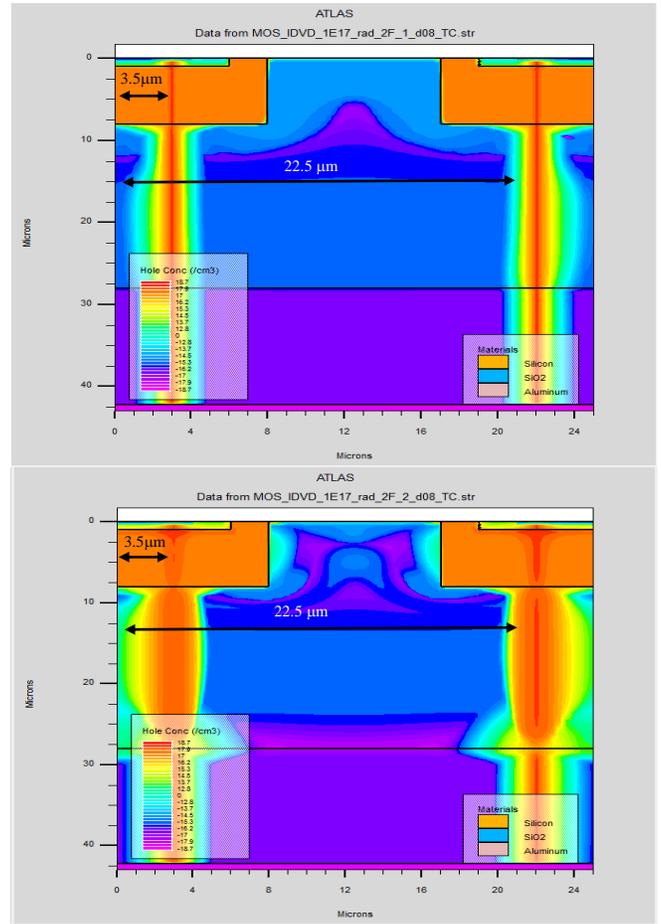


Fig. 7 - Beam of particle applied to the structure.

With the doping concentration increase in the drift region, at the incidence time of the beam, one can observe an increase in the peak of the drain current transient due to a greater number of carriers generated in this region. However, with the increased concentration of this region there is an increased of carriers recombination rate, Fig. 8, leading to a reduction in the drain current relaxation time.

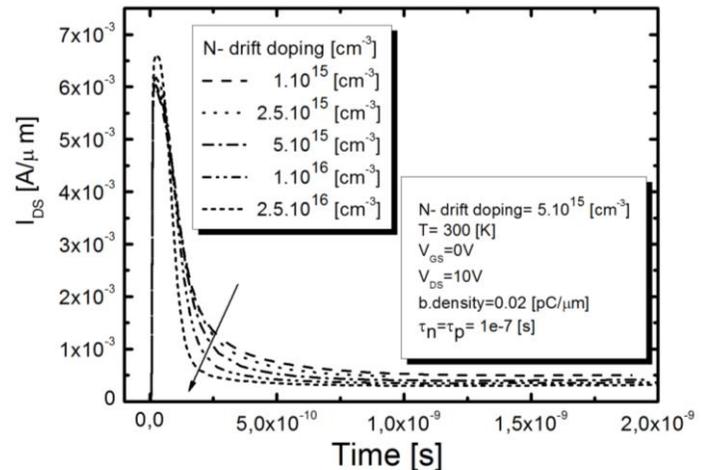


Fig. 8 - I_{DS} curve as function of time, with the doping concentration variation.

With increasing temperature there is a significant increase in the carriers recombination rate. This fact causes a lower

carries number that are captured by the drain, resulting in a reduction in the peak transient drain current, as observed through Fig. 9.

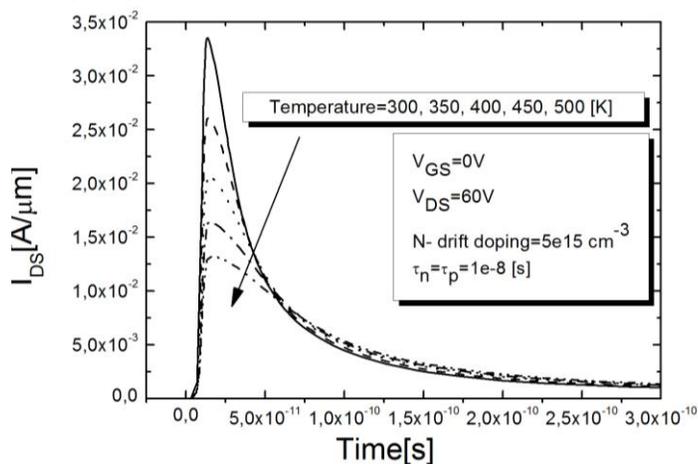


Fig. 9 - I_{DS} curve as function of time, with the temperature variation.

IV. CONCLUSIONS

In this work, the behavior of the breakdown voltage was analyzed in power MOSFET transistors. This analysis considered the influence of some technological parameters when these devices are under harsh environments. For higher temperatures the devices exhibited lower breakdown voltage, this fact is associated with the reduction of the impact ionization near of the drain region. On the other hand, for high temperature the power MOSFET showed less sensitivity to the radiation beam. With the doping concentration increase in the drift regions there was a significant reduction on the breakdown voltage, due to higher electric field values obtained in this case. A higher drain current transient with the doping concentration increase in the drift region was also observed after the exposure to the radiation beam. Finally, the influence that the carrier lifetime causes on the breakdown voltage was also analyzed. A reduced breakdown voltage can be achieved for larger lifetime carriers due to the enhanced current gain parasitic bipolar transistor. Additionally, it was observed a drain bias where there is not current variation with carrier lifetime.

ACKNOWLEDGMENTS

The authors would like to thanks the Centro Universitário FEI and SMS Power Electronics laboratory for the financial support.

REFERENCES

- [1] D.A. Grant and J. Gowar, "Power MOSFETs: Theory and Applications", Wiley, New York, 1989.
- [2] K.F. Galloway and R.D. Schrimpf, "MOS device degradation due to total dose ionizing radiation in the natural space environment: a review", *Microelectronic Journal*, Vol. 21 No. 2, 1990.
- [3] J.A. Felix, et al, "Effects of radiation and charge trapping on the reliability of high-j gate dielectrics", *Microelectronics Reliability*, Vol. 44, pp. 563-575, pp. 67-81, 2004.

- [4] J. P.COLINGE, "Silicon-On-Insulator Technology: Materials to VLSI", 3rd Edition, Boston, Kluwer Academic Publishers, 2004.
- [5] G. H. Johnson, et al. "A Review of the Techniques Used for Modeling Single-Event Effects in Power MOSFETs", *IEEE Transactions on Nuclear Science*, Vol. 43, No. 2, 1996.
- [6] Atlas. User's manual, Silvaco (2007).
- [7] B.J. Baliga, "Power Semiconductor Device Figure of Merit for High Frequency Applications", *IEEE Electron Device Letters*, Vol. EDL-10, pp. 455-457, 1989.
- [8] B. J. Baliga, "Fundamentals of Power Semiconductor Devices", Springer Science, 2008.
- [9] M. Galetti, et al, "Improved generation lifetime model for the electrical characterization of single and double gate SOI nMOSFETs", *Semicond. Sci. Technol.*, 23, 125011 2008.
- [10] J. Zeng et al., "An Ultra Dense Trench-Gated Power MOSFET Technology Using a Self-aligned Process", *IEEE International Symposium on Power Semiconductor Devices and ICs*, pp. 147-150, 2001.
- [11] SZE, S. M.: *Physics of Semiconductor Devices*, 2nd edition, New York: J. Wiley & Sons, 1981.