# Experimental investigation of THT and SMT power transistors under TID radiation

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***Abstract* — This research aimed to investigate, using experimental ways, the parameters variation of power MOSFET transistors of different packages, when exposed to X-Ray radiation. It was used transistors with similar electrical characteristics, however with a different packing. To determinate the transistors reactions it was conducted radiation sections with varied doses and the parameters were measured after a certain amount of time. The results showed a weaker SMT transistor under TID radiation, presenting larger parameters variations and even a rupture after a certain dose.**

***Keywords — MOSFET Transistors; Power MOSFET packing; Radiation on MOS transistors.***

## I - INTRODUCTION

Power MOSFETs has been widely used on modern power electronics [1-2]. This is justified because of its fast switching speed, and its ideal for various applications, like DC-AC converters, and the nMOSFETs transistors are widely use due the speed of the charge carriers [2-3].

Another important issue is related with the process by which components are mounted on the of printed circuit boards. The first technology invented was called through-hole (THT), where the electronic components presents leads that are inserted into the holes drilled in the printed circuit boards (PCB), and soldered to pads on the opposite side. The next generation, known as surface mount technology (SMT) the components are mounted directly on the surface of the PCB. The most obvious benefits of the SMT compared to older through-hole technology is increased circuit density and improved electrical performance, reduced process costs, higher product quality, reduced handling costs, and higher reliability. Fig. 1 presents the main difference between then [4-6].

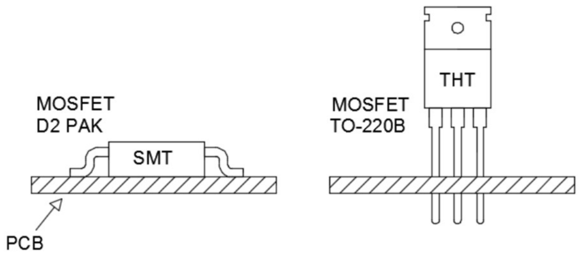


Fig. 1 – The different process used to mount the components on the PCB.

The two main types of packages used are the THT and the SMT and among them it was selected two of the most currently used: The D2 PAK (Fig.2 - a) and the TO-220AB (Fig.2 - b). The TO-220AB model uses the THT packing and has been widely used on the modern power electronics due its size, allowing a higher thermal dissipation [7]. On the other hand, the D2 PAK uses SMT packing and has lower dimensions, allowing the heat dissipation be done directly on the circuit board, and also presents a low input impedance, making them excellent for high frequency applications [7-8].

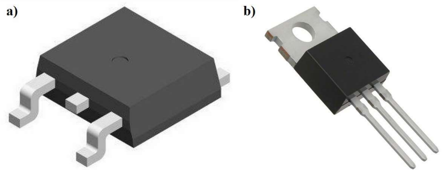


Fig. 2 – Packages: D2 PAK (a) and TO-220AB (b).

There were innumerous advances on modern microelectronics on the last years, like the development of new layouts and ICs internal structures [9], but something important to the performance of modern power circuits is the packing [10]. it changes a lot of transistors characteristics, among them are his inductance, decrease of his thermal performance and, mainly, his resistance to harsh environments, like high temperatures and the exposure to radiation (X-rays) [11]. In other words, despite the modern microelectronics advances, the packages ended up to limit the performance of MOSFETs [10].

Besides that, the effect of radiation on semiconductors has been widely research nowadays, due to advances on military and biomedical engineering [12]. Radiation refers to any physical processes of emission and propagation of energy, or by wave phenomena either by particles with kinetic energy. Ionizing radiation has a higher energy electron energy of binding of an atom with its nucleus, whose energy is enough to start their electron orbitals. The effects of radiation on MOSFETs can be divided as presented in Fig. 3.

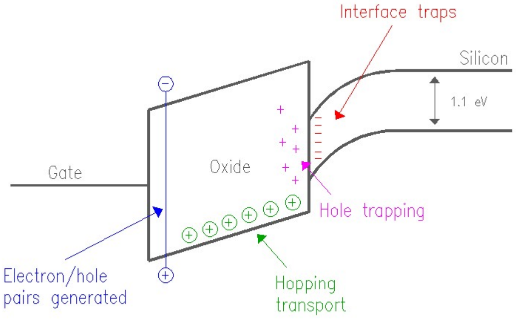


Fig. 3 – The ionizing effect on the MOSFET gate.

The effects of radiation on semiconductors can be divided into:

- Total Ionizing Dose (TID): this occurs when a high-energy particle focuses on the semiconductor structure, being absorbed by photoelectric effect. This is the main effect which causes changes on MOSFET parameters when exposed to radiation [12-13].

- Displacement damage: occurs when an incident particle kicks the silicon on the semiconductor structure out of his valence state and its changes electrical and optics characteristics [14].

- Single Event Effects: occurs when a single particle with high energy hits a single point on the semiconductor structure. These kinds of effects are more common on space environments; it is rare on land environments [15].

According to previous studies, the main effect of radiation on MOSFETs is his threshold voltage swift. The transistors show changes on his parameters on relatively low doses, and it can cause permanent failures on sensitive devices [16].

## II - EXPERIMENTAL SETUP AND DEVICE CHARACTERISTICS

To expose the MOSFETs to X-ray radiation it was used the Shimadzu XRD-7000 diffractometer (Fig. 4), with dose rate of 5.75 krad/min. The devices were exposed for 18 minutes, creating a 100 krad total dose, which was accumulate during the study. The diffractometer also provides an effective energy of 10 keV with a 10 mA source. It is worth nothing that it was not made to correct the total dose of radiation absorbed by the epoxy coverage of the devices, but it is estimated that only 20% of the total radiation dose value has really hit the device.

The chosen MOSFETs were selected to be the most common commercially on the power electronics area, and they also needed to have similar electrical characteristics. Tab. 1 presents the main parameters extracted from the datasheet.

For the characterization it was used the Semiconductor Characterization System Keithley 4200. The electrical measures were made about a week after the exposure. It was observed how much the devices reacted to the doses, aiming to compare the packages between them.

Tab. 1 – Chosen MOSFETs for the study.

| Device | Description | Manufacturer |
|---|---|---|
| IRF540N<br>(THT) | nMOSFET<br>33A<br>100V | International Rectifier |
| IRF540Z<br>(SMT) | nMOSFET<br>36A<br>100V | International Rectifier |

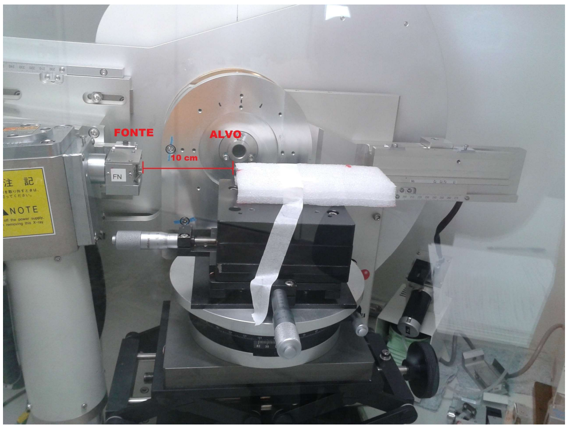


Fig. 4 – Shimadzu XRD-7000 diffractometer used to radiate the MOSFETs.

## III - RESULTS AND ANALYSIS

### *A – Threshold voltage*

The threshold voltage ($V_T$) was extracted through second derivative method, as shown in Fig. 5 [17]. An increase on $V_T$ could be observed for THT devices, although for SMT one the opposite behavior is shown. The accumulation of positive charges trapped in the oxide creates a vertical electric field at the surface of the substrate by attracting electrons to the silicon / oxide interface. The attracted negative charges decrease the concentration of positive charges near the surface of the substrate, which makes it easier to reach the threshold inversion of the substrate, and the visible effect would be to reduce the threshold voltage. Another alternative is the presence of loads at the interface between silicon and gate oxide that could cause this increase on the threshold voltage

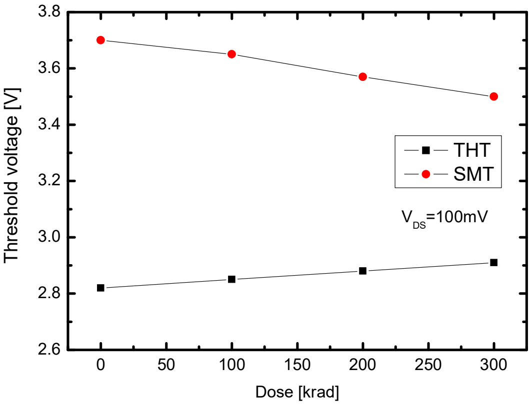
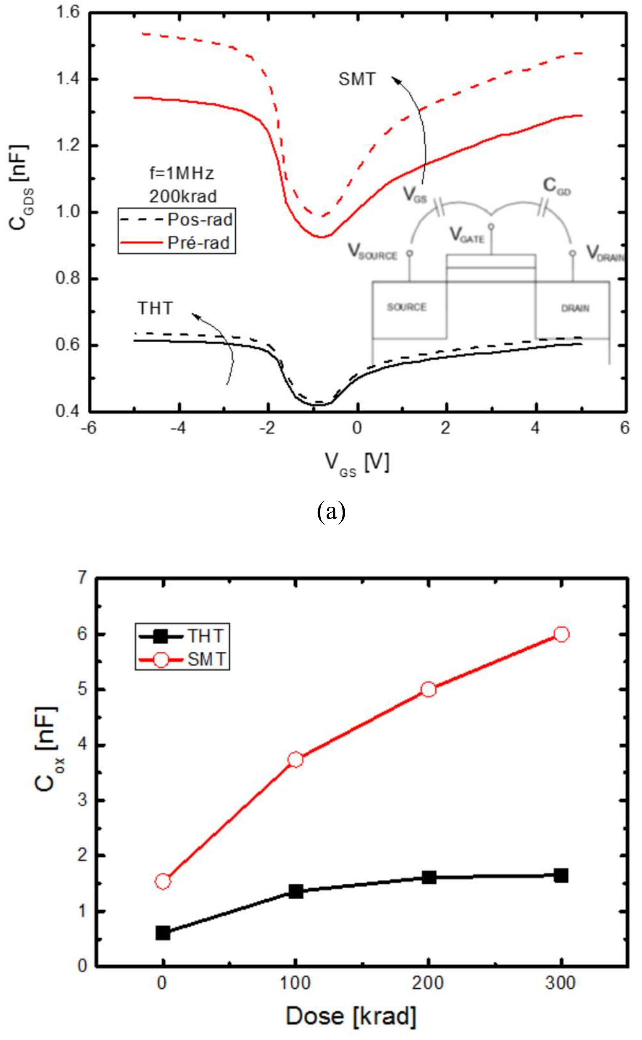


Fig. 5 – Threshold voltage extracted for different radiation dose on both package.

### *B - Gate do drain/source to gate capacitance*

The behavior of the capacitance between drain/source to gate depending on the gate voltage was also analyzed, as shown in Fig. 6 below. The measurement was performed between the gate and drain/source electrodes as shown in the inside of the picture with a high frequency 1MHz. Initially, that is possible to observe that SMD package presents larger capacitance. Moreover, the device when spouse to X-Ray can present a reduced gate to drain capacitance.

The gate oxide capacitance ($C_{ox}$) was extracted at the maximum point of the curve (at $V_{GS}$=-5V). For both packages, when the device is exposed to X-Ray an increase on $C_{ox}$ is seen. Although, devices with SMD package indicate a larger variation on $C_{ox}$.



(a)

(b)

Fig. 6 – (a) Gate do drain/source capacitance and (b) gate oxide capacitance as a function of radiation dose.

Fig. 7 presents the bond wires difference between TO220 and $D^2$PAK package. TO220 presents low resistance (Rth) when mounted to a suitable heatsink, but the bond wires give significant package resistance, high inductance, poor drain current, and thermal performance unless a heatsink is used.

$D^2$PAK is a surface-mount variant of the TO220 package. The transistor is assembled in the same manner to TO220, but the drain tab and the gate and source pins are modified to make the device suitable for surface mount and reflow soldering directly to a printed circuit board. D2PAK package presents lower package resistance and inductance than TO220 since the drain connection is made via the power-tab instead of TO220 lead [18]. As a result, improved electrical performance usually appears as higher operating speed and frequency for $D^2$PAK package. Additionally, surface mounting components shown lower parasitic lead and conductor inductance while improved capacitance, resistance and other performance characteristics.

Fig. 7 – Die package configuration for TO-220 (left) and $D^2$PAK (right).

### *C - Breakdown voltage*

The breakdown voltage ($B_V$) is the maximum voltage that the transistor can withstand without damage. From this voltage begins to increase the current between the source and the drain avalanche process, while the gate and the source are short circuited. Fig. 8 shows the drain current as a function of the drain bias for a zero voltage at the gate for THT devices with different dose rate. At the voltage of the abrupt increase on the drain current, it is possible to estimate the breakdown voltage that is around 115 V been in agreement with the datasheet of the devices. A small increase on $B_V$ was observed as the dose rate is increased (around 1.4% for 300 krad). On Fig. 9 is shown the breakdown voltage behavior for SMT devices with and without radiation. As observed before an increase is seen, but larger than THT devices (around 15.2% for 300 krad).

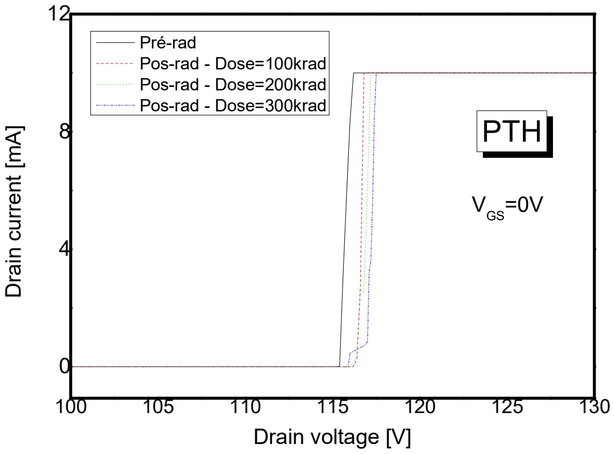


Fig. 8 – Breakdown voltage behavior for THT.

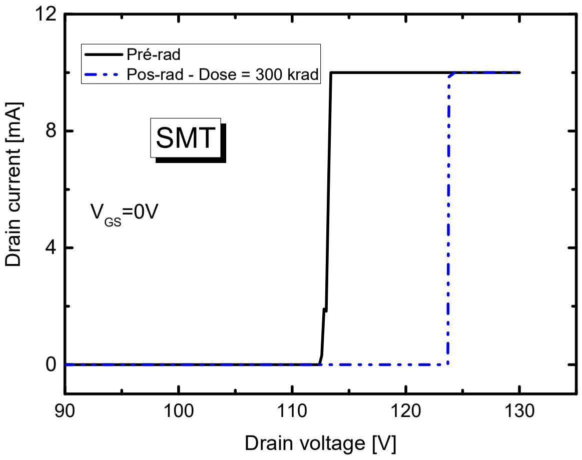


Fig. 9 – Breakdown voltage behavior for SMT.

## III - DISCUSSION

An increase in the threshold voltage was also observed, because the ionizing radiation exposure can induce accumulation of charges at the oxide/silicon interface. Due to TID effect, loads are trapped that produces electrostatic effects causing the deviation of the threshold voltage. This deviation is given by the accumulation of positive charges trapped in the interface, causing the increase of concentration of positive charges on the substrate surface, which makes it harder to reach the threshold for inversion of the substrate. As a result of the increase in threshold voltage, it was also observed an increase in the breakdown voltage of the power transistors when subjected to radiation.

## IV - CONCLUSIONS

The SMT packages seems to suffer more when exposed to TID radiation, according with the measures and parameters extracted. It shows that the D2 PAK is weaker than the TMT, probably because of his construction and thin layer. The results also showed some know characteristics about the TID effect on nMOSFETs, like the swift on the threshold voltage and an increase on breakdown voltage.

## ACKNOWLEDGMENT

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