Study of the Invariant Point with the Carrier Lifetime in Power MOSFET Transistors

A. C. Reis and M. Galeti[1]

[1]Centro Universitário da FEI - São Bernardo do Campo, Brasil

e-mail: amandacreis@hotmail.com

ABSTRACT

This work aims to study the invariant point with the carrier lifetime in power MOSFET transistors. The influence of the technological parameters, such as dopant concentration and the carrier lifetime were studied, as well as the effect of temperature. During the analysis of the devices characteristic curves were observed two invariant points that presented dependency with the parameters analyzed. The behavior of these invariant points with the variation of the carrier lifetime was studied as a function of the temperature and the doping concentration.

Index Terms *— Power MOSFETs, Invariant Point, Carrier Lifetime, Breakdown Voltage.*

I. INTRODUCTION

The significant growth of applications in power electronics areas, the need for improvements, it open space for the use of new technologies capable of improving equipment efficiency with the size reduction [1]. MOSFET (Metal-Oxide Silicon Field Effect Transistor) is becoming the most widely used device, especially in the design of integrated circuits (IC's), which are manufactured on a silicon wafer [2]. Even with the increasing advances in the area of microelectronics, from the point of view of the manufacturing process of power devices, we have not yet obtained solutions that allow the amplification of the applications of these devices in terms of voltage blocking and current conduction, being limited to the capacity of silicon [3]. In applications such as power electronics, it is essential to operate these devices at high switching frequencies, such as DC-AC converters, so these devices must operate at reduced losses during the switching process. In addition, semiconductor devices used in high power systems must withstand high currents and voltages as well as high reverse voltages during their switching [4]. Due to the need for continuous improvement of the technology, always seeking a better performance, it is necessary to study the operation of these transistors in the lock mode. In this mode of operation, the drain junction breakdown voltage defines the reverse voltage that these devices are able to withstand. Some technological parameters such as dopant concentration and carriers lifetime influence this parameter, as well as the exposure of these devices to severe environments [5,6]. This work has as main focus of interest the point of polarization of the drain in which the device doesn't present variation in the drain current with the variation of the carrier lifetime when operating in lock mode.

II. NUMERICAL SIMULATIONS

MOSFET structure cross-section is shown in Figure 1. Two-dimensional numerical simulations using the Atlas (SILVACO) [7] were performed, including recombination, impact ionization, photo-generation, energy band narrowing and carrier lifetime models. In addition, it was incorporated the Boltzmann and Fermi-Dirac statistics, including the incomplete ionization of impurities with the aim of making the results more accurate. The power MOSFET transistors analyzed in this work were simulated with the parameters presented in Table 1.

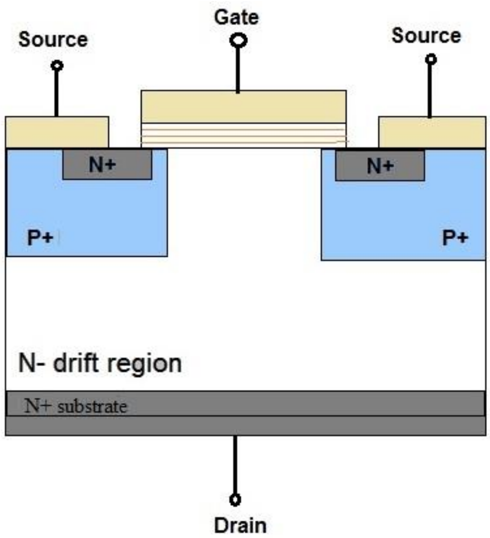

Fig. 1 – Schematic cross-section of a Power MOSFET transistor.

TABLE 1

MOSFET STRUCTURE PARAMETERS USED IN THE SIMULATIONS.

Parameter	Value	Unit
N+ Thickness (Drain)	15	µm
Concentration Region N+ (Drain)	1.10^{20}	cm^{-3}
N- Drift Region Thickness	27	µm
Drift Region Concentration	$1.10^{15} – 1.10^{16}$	cm^{-3}
N+ Source Region Thickness	1	µm
Concentration Region N+ (Source)	1.10^{20}	cm^{-3}
Port Oxide Thickness	0,04	µm
Channel Region Length	2	µm
P+ Concentration of the Canal Region	1.10^{17}	cm^{-3}
Carrier Lifetime	$0,7.10^{-7} – 5.10^{-7}$	S

The breakdown voltage of a power semiconductor device is one of its most important characteristics. Together with its maximum current, this parameter determines the power rating of the device [8]. Figure 2 shows the schematic that illustrates the extraction of breakdown voltage from the I-V behavior of the power MOSFET during the operation in the blocking mode, V_{GS}=0V.

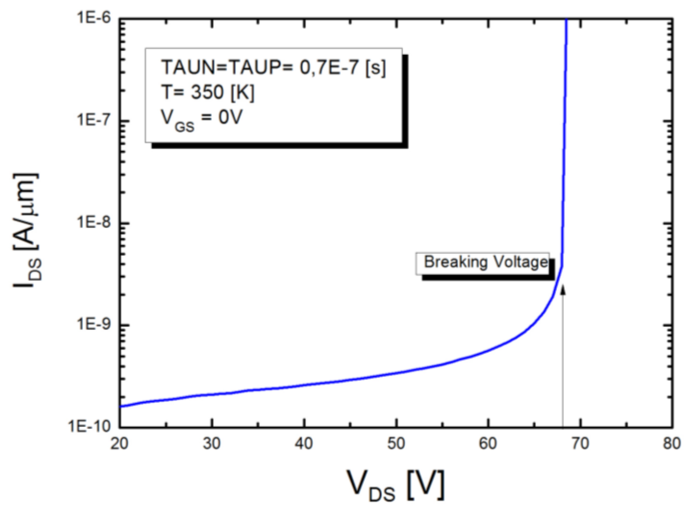

Fig. 2 - Illustration extraction of the breakdown voltage.

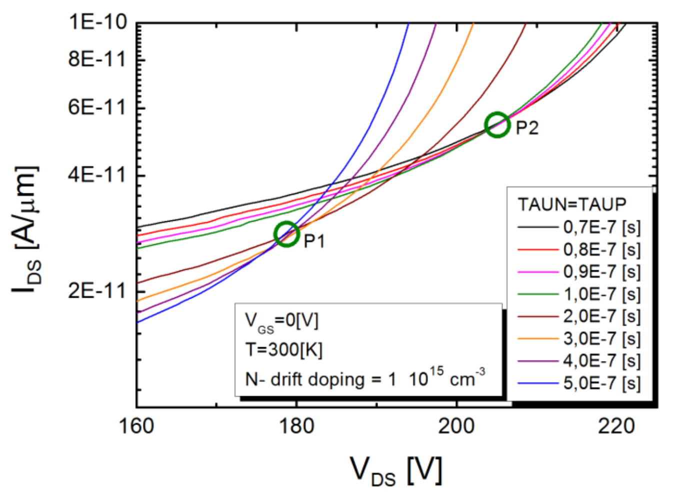

Fig. 3 - I_{DS} versus V_{DS} curves with the carrier lifetime variation.

III. SIMULATIONS RESULTS

A. Technological Parameters

Figure 3 shows the drain current curves (I_{DS}) as a function of the drain voltage (V_{DS}) with the change in the carrier lifetime. The drain current during operation in blocking mode (V_{GS}=0 V) can be calculated by Eq. 1 [9]:

$$I_{leak} = qA\left(\frac{D_n}{\tau_n}\right)^{\frac{1}{2}} \frac{n_i^2}{N_a} + qA\frac{n_i W}{\tau_e} \qquad (1)$$

Where q is the electron charge, A is the junction area, D_n is the electron diffusion coefficient, τ_n and τ_p is the electron and hole lifetime, n_i is the intrinsic carrier concentration, N_a is the doping concentration, W is the depletion width of and $\tau_e = (\tau_n + \tau_p) / 2$ is the effective lifetime.

With the increase in the carrier lifetime (τ_n) there is a reduction in the leakage current level of the MOS structure for the same doping concentration, according with Eq.1. The breakdown voltage reducing that occurs with increasing the carrier lifetime is attributed to the increase in gain (β) of the parasitic bipolar transistor inherent in the MOSFET structure, formed between the N+ source region, the P-base and the N-drift region [10,11]. Due to these two associated effects appear two cross point in the drain current curve (I_{DS}) as a function of the drain voltage (V_{DS}), as highlighted in the fig. 3. Point 1 (P1) is caused by curves referring to carrier lifetimes of 2 10^{-7} to 5 10^{-7} cm^{-3} and the point 2 (P2) of 0.7 10^{-7} to 1 10^{-7} cm^{-3}.

B. Temperature

Figure 4 shows the I_{DS} as a function of the V_{DS}, with the temperature variation from 350, 400, 450, 500 and 550K, N = 5.10^{15} cm^{-3}. It can be observed that the drain current during operation in blocking mode (V_{GS}=0 V) is strongly influenced by temperature variation due to the dependence of this current with the intrinsic concentration. Despite the leakage current increase for higher temperatures, the breakdown voltage is increased due to reduction in carrier mobility which decreases the impact ionization near of the drain region.

For each temperature simulation, leakage current values were extracted adopting a fixed voltage that contemplated all the currents in the region of parallelism. For the breakdown voltage, a similar methodology was adopted where the current value was set to extract the breakdown voltage. These values are changed according to the corresponding temperature. For example, Figure 4 shows the simulation with T = 400K, breakdown voltage of 40V and leakage current of 1.2 10^{-7} A/µm. And also the value of each taun=taup curve has a different value of breakdown voltage.

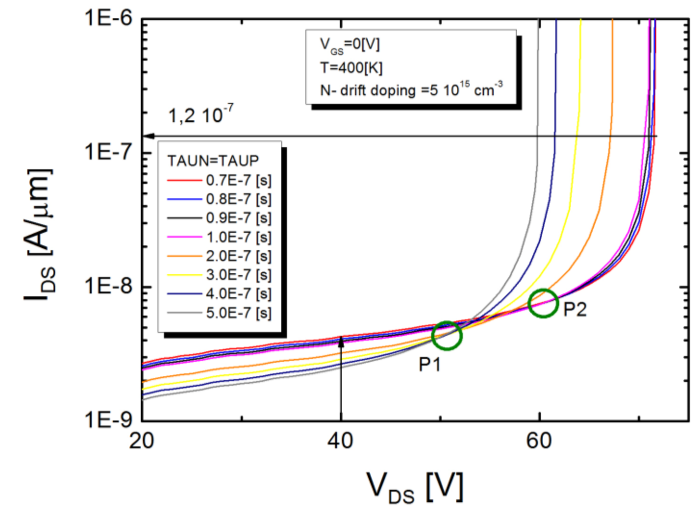

Fig. 4 - I_{DS} versus V_{DS} curves with the carrier lifetime variation for temperature of 400 [K]

Figure 5 shows the average behavior of the invariant points in relation to the temperature variation. We can observe that with increasing temperature the drain voltage where it occur the cross point remains almost constant. This behavior can also be seen in the Table 2. This observed behavior is valid for both points (P1) and (P2) as can be observed through the Δ_{VDP2} - Δ_{VDP1} seen in Fig. 6.

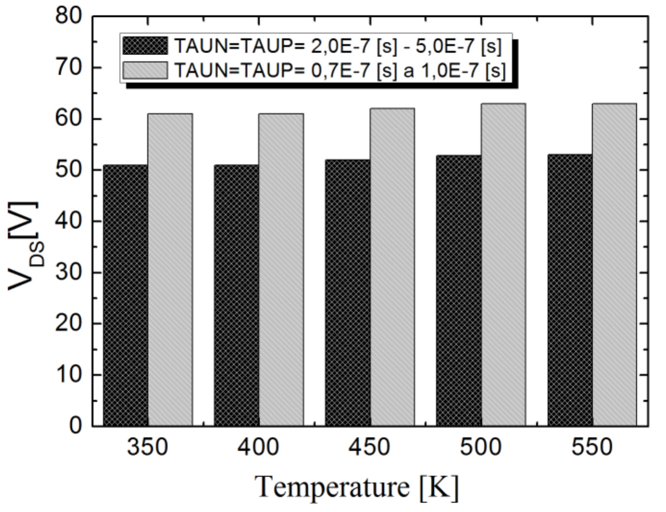

Fig. 5 – Average behaviour of the cross point as a function of the temperature.

TABLE 2

MEAN BEHAVIOR OF THE INVARIANT POINT ACCORDING TO TEMPERATURE VARIATION.

Temperature [K]	**Point 1 [V]**	**Point 2 [V]**
350	51	61
400	51	61
450	52	62
500	52,8	63
550	53	63

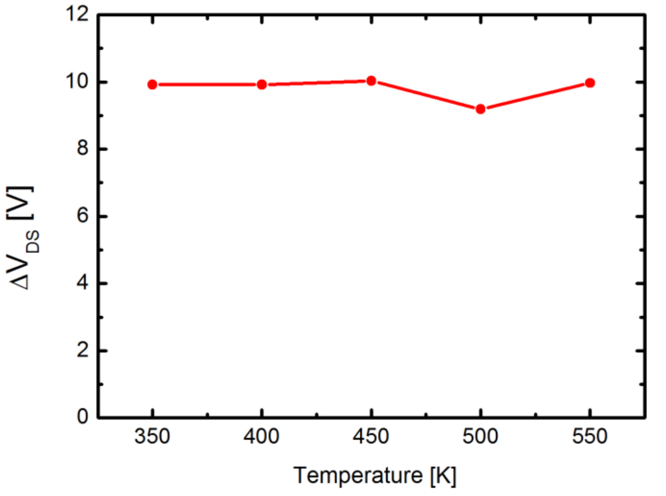

Fig. 6 - Voltage variation of the cross point as a function of the temperature.

The extracted data suggest that the carrier lifetime influence occurs in a similar way for both the parasitic bipolar transistor gain and the leakage current when there is temperature change, Fig.7.

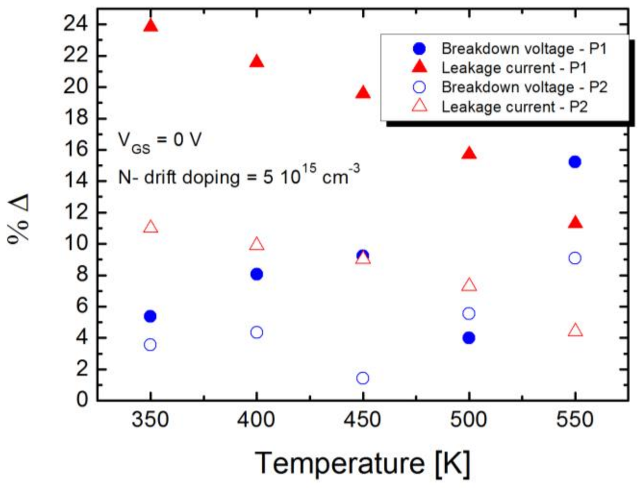

Fig. 7 – Variation of the breakdown voltage and leakage current as a function of the temperature.

C. Variation of Lifetime in Concentration

The simulations presented in this section were performed with V_{GS}=0V (blocking mode), temperature T = 300K, and doping concentration in the range of 1.10^{15} cm^{-3} to 1.10^{16} cm^{-3}. According to Figure 8 shows the average behavior of the invariant points in relation to the variation of dopant concentration. It was verified that when the concentration of dopants increases in the drift region, the drain voltage (V_{DS}) that occurs the cross points is smaller, this fact can be verified also through Table 3.

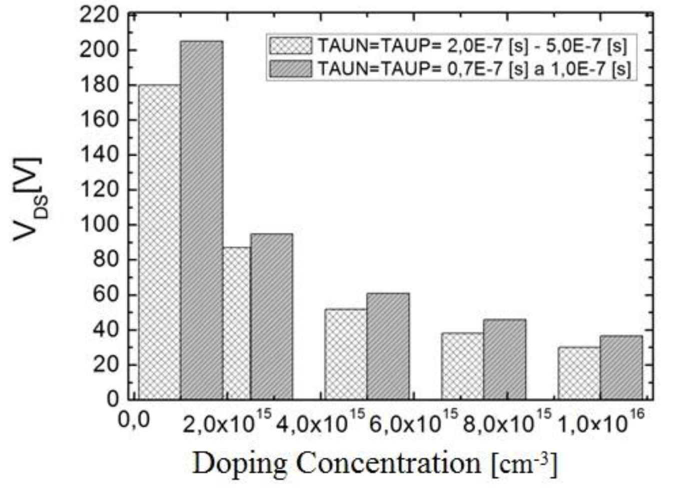

Fig. 8 - Mean behavior of invariant points as a function of the doping concentration.

TABLE 3

AVERAGE BEHAVIOR OF THE INVARIANT POINT ACCORDING TO THE VARIATION OF DOPING CONCENTRATION.

Concentration [cm^{-3}]	Point 1 [V]	Point 2 [V]
1E15	180	205
2,5E15	87	95
5E15	52	61
7,5E15	38	46
1E16	30	36,6
2,5E16	14,6	18,3

With the increase in the carrier lifetime, there is a reduction of the breakdown voltage due to the increase in the gain of the parasitic bipolar transistor, in addition, we realize that the leakage current decreases with increasing lifetime.

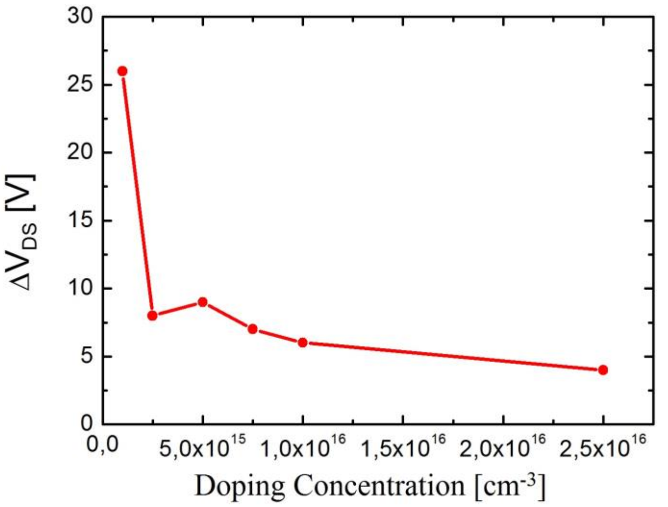

Fig 9 - Variation of the rupture voltage and the leakage current in relation to the concentration.

When there is doping concentration variation in the drift region, a greater percentage variation was observed in the leakage current than in the breakdown voltage, fig.10, which justifies a decrease in the Δ shown in Fig. 9. This suggests that for higher doping concentrations the influence of the carrier lifetime in the leakage current is more significant than in the gain of the parasitic bipolar transistor.

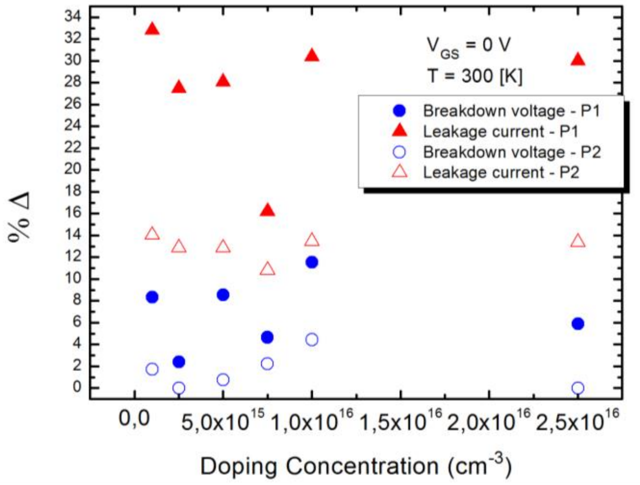

Fig 10 - Voltage variation of the points in relation to the concentration.

IV. CONCLUSIONS

It is possible to conclude that the variation of some technological parameters of the power MOSFET transistor influences the behavior of the invariant point, emphasizing that this behavior was analyzed in blocking mode (V_{GS} = 0V). The first result observed with the temperature variation (350K to 550K) along with the carrier lifetime was the presence of two invariant points. These points are determined by a drain voltage value that the drain current is constant with the carrier lifetime variation. The behavior these points were studied with the temperature and the doping concentration variation. With the temperature variation, the difference of the voltage at which these two points occur remained constant ($\Delta V_{DS} = V_{DSP2} - V_{DSP1}$).

The second result observed at the cross point position was with the doping concentration variation (1.10^{15} cm^{-3} at 1.10^{16} cm^{-3}). The increase in the doping concentration of the drift region leads to a reduction in ΔV_{DS}. The percentage variation suggests that the carrier lifetime influence is greater in the leakage current than in the parasitic bipolar transistor gain for higher concentrations of the drift region.

V. ACKNOWLEDGMENTS

The authors would like to thanks the Centro Universitário FEI for the financial support.

VI. REFERENCES

[1] Mohan, Undeland, Robbins. Power electronics: converters, applications and design, Wiley, India, 2007.

[2] B. J. Baliga, “Fundamentals of Power Semiconductor Devices”, Springer Science, 2008.

[3] Almeida, J. L. A. Semiconductor Devices: Thyristors: Power Control in C.C and C.A. Ed. Érica, 1996.

[4] Schroder, D. K.; Semiconductor Material and Device Characterization, New York, John Wiley & Sons.

[5] B.J. Baliga, “Power Semiconductor Device Figure of Merit for High Frequency Applications”, IEEE Electron Device Letters, Vol. EDL-10, pp. 455–457, 1989.

[6] G. H. Johnson,et al “A Review of the Techniques Used for Modeling Single-Event Effects in Power MOSFETs”, IEEE Transactions on Nuclear Science, Vol. 43, No. 2, 1996.

[7] Atlas. User’s manual, Silvaco (2007).

[8] J. P.Colinge, “Silicon-On-Insulator Technology: Materials to VLSI”, 3nd Edition, Boston, Kluwer Academic Publishers, 2004.

[9] SZE, S. M.; Physics of Semiconductor Devices, 2nd edition, New York: J. Wiley & Sons, 1981.

[10] M. Galeti, et al, “Improved generation lifetime model for the electrical characterization of single and double gate SOI nMOSFETs”, Semicond. Sci. Technol., 23, 125011 2008.

[11] J. Zeng et al., “An Ultra Dense Trench-Gated Power MOSFET Technology Using a Self-aligned Process”, IEEE International. Symposium on Power Semiconductor Devices and ICs, pp. 147–150, 2001