Experimental study of FD and PD SOI nMOSFET with and without HALO.

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ABSTRACT

In this work, the behavior of partially (PD) and fully (FD) depleted MOSFET were experimentally analysed through basic parameters. The subthreshold slope (SS), threshold voltage (Vth) and transconductance (gm) were extracted considering several gate lengths and devices with and without HALO structure.

KEYWORDS AND PHRASES

SOI nMOSFET; Fully and Partially Depleted; Basic Parameters

1 INTRODUCTION

With the aggressive reduction of devices dimensions, the MOSFET technology is suffering too much with short channel effects (SCE). Then, the bulk MOSFET has been replaced by the Silicon On Insulator (SOI) technology. In addition, the CMOS technology of 130nm uses the HALO structure to improve the SCE [2].

The HALO implantation can be made by several ways, one of them is to do a tilted implantation and lateral diffusion of silicon self-interstitial during oxidation after the gate patterning enhance the diffusion of the channel dopant. This phenomenon results in non-uniform lateral distribution of the channel dopant. One secondary effect is that the threshold voltage of halo devices increases for shorter channel lengths [2].

The SOI transistors can be classified depending on the silicon film thicknesses (tSi) and channel doping concentration. The thin silicon film transistor (where tsi < Xdmax) is classified as a fully depleted, while for thick Si film (where tsi > 2.Xdmax) is a partially depleted one [3].

The aim of this work is study the SOI technology for both PD and FD transistors and for the last case with and without HALO structure. This analysis was performed for several channel lengths (from 10□m down to 300nm).

2 EXPERIMENTAL DETAILS

The studied devices were fabricated at Imec on (100) SOI substrate with the following characteristics: the gate and buried oxide thicknesses (t_{OXF} and t_{OXB}) are 2.5nm and 390nm, respectively. For partially depleted devices, there was no Halo structures, the silicon film (tSi) is 100nm and the channel doping concentration (Na) is 5.5x1017cm-3, while for fully depleted one tSi is 30nm and Na is 1x1018cm-3. For both PD and FD devices, the channel length varies from 10µm down to 300nm. Figure 1 shows a schematic SOI nMOSFET. More details can be found in [5].

All the DC measurements were performed with the grounded substrate (VB) for three dies. The used parameter analyzer was B1500 from Keysight.

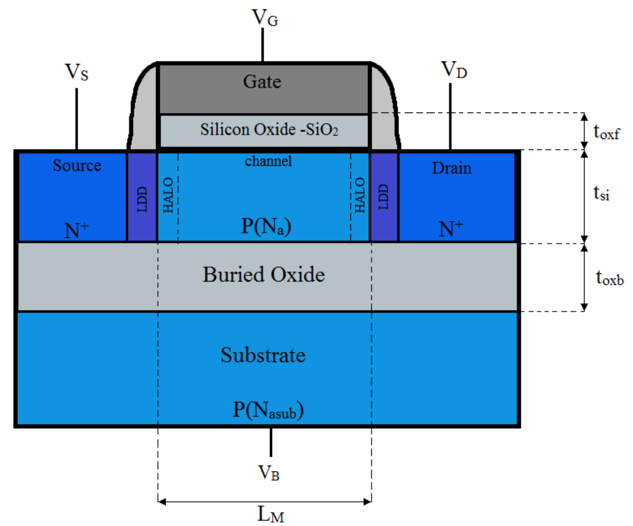

Fig 1. Cross-section of a SOI nMOSFET

3 RESULTS AND DISCUSSION

The drain current characteristics (I_D) as a function of gate voltage (V_G) is shown in the figure 2, for a channel length of 800nm for three different wafers.

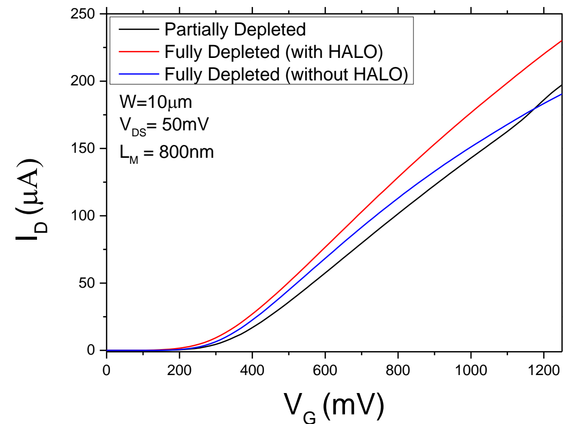

Fig 2. Drain current as a function of front gate voltage for V_D=50mV for three different devices (PD, FD with and without HALO).

As observed, the FD transistors has a smaller threshold voltage (Vth) in comparison to the PD one. This is because of the Fully

Depleted present lower depletion charge. Both FD transistors present almost the same Vth value.

The figure 3 shows the threshold voltage (Vth) behavior, obtained by the second derivative method. On partially depleted devices, it is noted a slightly Vth reduction for channel lengths smaller than 600nm. For fully depleted devices, two opposite behaviors are observed. The transistors with HALO presented an increased Vth for channel lengths shorter than 300nm, while the FD without HALO did not have a significant variation for the measured channel lengths. It occurs because the devices with HALO present a higher effective channel concentration for shorter channel lengths.

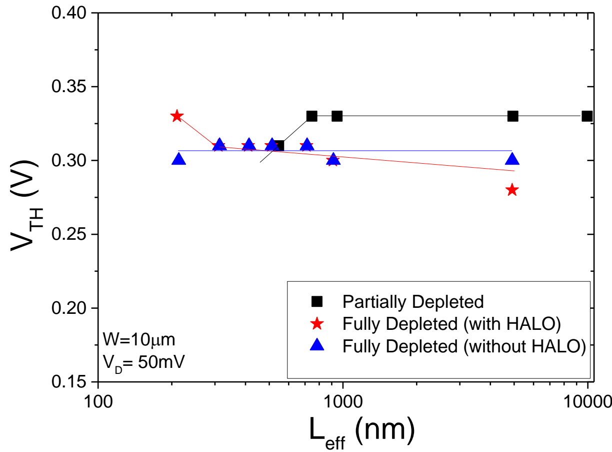

Fig 3. Threshold voltage by effective channel length for V_D=50mV for three different devices (PD, FD with and without HALO).

Then, comparing all the behaviors, it is noted that, for PD devices, a slightly variation was observed, showing that for L_{eff} ≥600nm, no SCE occurs. But the tendency indicates that it starts to occur for devices shorter than this limit.

On FD devices, due to a thinner tsi, it's not observed SCE for transistor without HALO. However, for devices doped with HALO, a reverse short channel effect (RSCE) is observed for channel lengths shorter than 300nm due to the higher effective doping concentration, i.e., it requires a greater gate voltage (V_G) to invert the channel.

Figure 4 presents the maximum transconductance values for all the measured channel lengths, with PD and FD transistors operating in triode.

In the graph, it is noticed that the maximum transconductance (gm_{max}) increases as the channel length reduces, what is expected by the ratio of the channel length, which occurs inversely with the transconductance.

This relation can be viewed in the equation (1)

$$gm = \mu_N C_{OX} V_D \frac{W}{L} \quad (1)$$

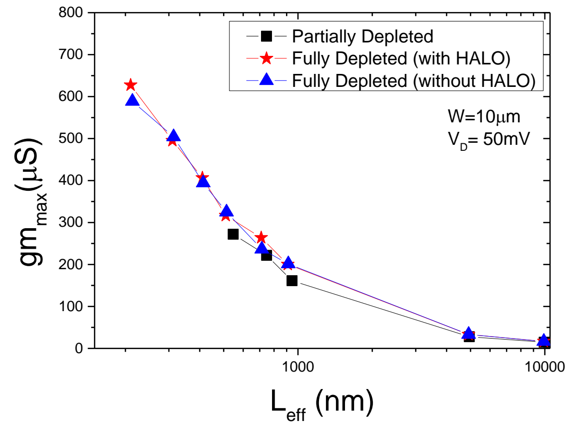

Fig 4 Transconductance as function of channel length for V_D=50mV for three different devices (PD, FD with and without HALO).

The gate oxide capacitance (C_{OX}), the width (W) and the drain voltage (V_D) are kept constant, changing only the channel length of the transistors, manufactured in the same Silicon On Insulator wafer.

The maximum transconductance (gm_{max}) were also used to extract the effective channel lengths (Leff). Figure 5 shows the inverse of maximum transconductance ($1/gm_{max}$) as function of all mask lengths (LM). The linear extrapolation method was used to obtain ΔL, and then, each effective length could be found by the equation (2).

$$L_{eff} = L_M - \Delta L \quad (2)$$

In the figure 5, it can be observed how the method was applied, and the values of each ΔL for PD and both FD transistors.

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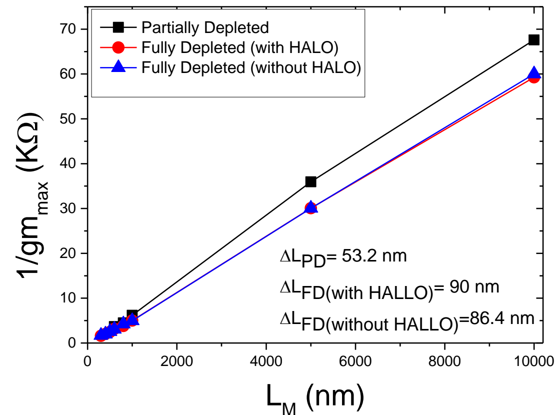

Fig 5. Inverse of the maximum transconductance as function of mask channel length for V_D=50mV for three different devices (PD, FD with and without HALO).

In order to analyze the transconductance behavior, excluding the channel length influence on the transconductance value, the gm_{max} was normalized multiplying by ($gm*L_{eff}$). Figure 6 shows the normalized transconductance as a function of effective channel length for the three different studied structures.

From figure 6 it is possible to note that both FD devices present a higher transconductance than the PD one. It can be explained by two different factors: the higher coupling between the gate and the channel, and the higher effective mobility. Short channel devices (L_{eff} <600nm) present an abrupt degradation of the maximum transconductance value caused by the short channel effects (loss of gate voltage V_G control over channel charges).

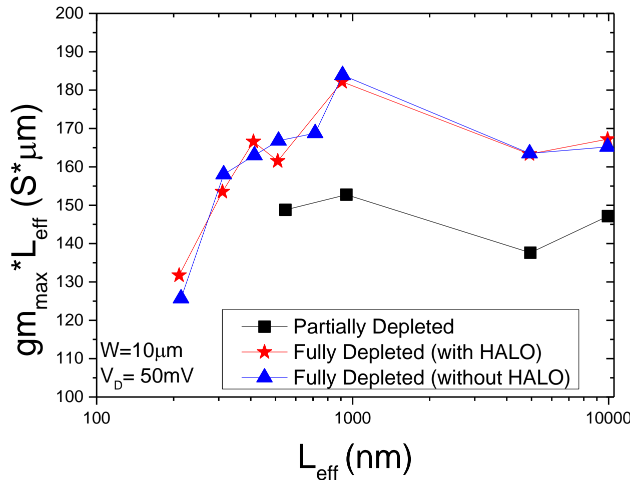

Fig 6 Normalized transconductance as function of effective channel length for V_D=50mV for three different devices (PD, FD with and without HALO).

Figure 7 shows the subthreshold slope (SS) as a function of the effective channel length. As can be observed on SS graph, there is not a significant variation as the channel length is reduced, all values are between 60 and 70 mV/dec.

It is possible to note higher values of SS for PD devices (as expected) and, on FD transistors, for the shorter channel length, it is possible to note the beginning of the SCE. For lengthy channels, the FDs present a SS near to the ideal value.

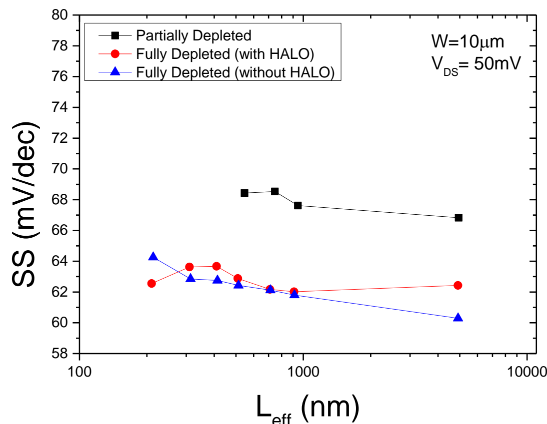

Fig 7. Subthreshold swing as a function of effective channel length for V_D=50mV for three different devices (PD, FD with and without HALO).

4 CONCLUSIONS

The FD devices presented a better short channel effect (SCE) control in comparison to the PD one. It was verified that SCE for FDs without HALO occurs a little bit earlier than for FDs with HALO due to the higher effective concentration for short channel devices, which in fact cause a reverse SCE. For FD devices the SCE occurs for channel lengths shorter than 300nm while, for PD, it occurred to channels shorter than 600nm.

The transconductance presented an increase as the channel was reduced, respecting its inverse relation with the effective channel length. Its was also verified the influence of the effective channel length using the normalized transconductance and it was observed the SCE for channel lengths shorter than 300nm for FD devices.

In the subthreshold slope curve, a higher value of SS was observed for PD devices till 600nm of channel length. However, for FD devices it is possible to observe just a beginning of the SCE since for the smallest studied channel length the SS values tends to increase for FD without HALO.

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REFERENCES

[1] Sedra, Adel S., Smith, Kenneth C.; "Microeletrônica" – São Paulo, Makroon Books – vol. 4 p338 – 2004.

[2] T. Kunikiyo ; K. Mitsui ; M. Fujinaga ; T. Uchida ; N. Kotani "IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS", VOL. 13, NO. 4, APRIL 1994.

[3] COLINGE, Jean P, SILICON-ON-INSULATOR TECHNOLOGY: MATERIALS TO VLSI 3rd Edition

[4] MARTINO, J. A. PAVANELLO, M. A., Verdonck, P. "Caracterização elétrica de tecnologia e dispositivos MOS".

[5] AGOPIAN, P. G.; MARTINO J. A.; SIMOEN E.; CLAYES, C. "Temperatura influence on the gate-induced floating body effect parameters in fully depleted SOI nMOSFETs", 2008.