# Electromagnetic Simulation and Analysis of Crosstalk Effect in Integrated Circuits

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## ABSTRACT

The electromagnetic interaction between two near lines in integrated circuits is a key factor for modern high-frequency and high-power circuits. The analysis of the physical parameters that affect crosstalk effect in integrated circuits and its equivalent electrical model are both herein presented. The work was developed through computer electromagnetic simulation in a CMOS 130 nm fabrication process. Several geometries and layout configurations for near signal coupling were used. Parameter variations for crosstalk improvement and worsening between two parallel lines were evaluated. An electric model for the coupling effect was validated, and a method for parameter extraction is proposed.

## Categories and Subject Descriptors

B.7.0 [**Integrated Circuits**]: General

## Keywords

Crosstalk Effect, Transmission Lines, Electromagnetic Simulation, Electrical Modeling

## 1. INTRODUCTION

The size downscaling of modern integrated technologies and their growing integration complexity make the electromagnetic interaction between adjacent regions an increasingly important aspect. Such factors lead to closer signal paths and at the same time longer interconnections. Combining these characteristics with the demanding integration of high-frequency and high-power blocks (as in integrated transmitter power amplifiers), the capacitive and inductive parasitic effects inside the chip present high influence on circuits performance [4]. These aspects constitute the crosstalk effect, which results from the coupling between two or more conductors for time varying signals [7].

In this paper a simulation analysis and a simulation-based electrical modeling of the crosstalk effect between two adjacent RF signal paths are presented. The paper is organized as follows: Section 2 shows a review about the coupling effect. In Section 3, the methods for the evaluations and experiments are presented. Simulation results of the analysis and the equivalent electrical models are shown in Section 4 and Section 5 presents the concluding remarks.

## 2. CROSSTALK EFFECT

The loading delay between various points of a strip line is decisive for the performance of high speed circuits. The interconnections can not be considered as short circuits and their transmission line (TL) behavior inside integrated circuits is therefore adopted. This approach has been adopted since subnanosecond applications started [2]. All effects regarding the transmission behavior can be represented using a lumped circuit model. The transmission line is divided in small elements of length $\Delta z$ with an associated discrete circuit to represent its impedance, as described in [6].

One of the effects regarding the transmission lines is the crosstalk. This phenomenon is common in printed circuit boards and in cables for high-speed signals due to the their size. In integrated circuits it can be present because of the high proximity between the lines and the existence of several near layers of conductors and insulators causing the occurrence of parasitic capacitances with common terminals (usually the ground). This effect tipically causes undesired consequences on circuit performance like interference and signal degradation. For this reason sometimes it can be refered as crosstalk "noise" [3]. Also, the usual nomenclature for the associated lines is "aggressor" for the line with the main signal and "victim" for the nearby affected line [7, 3].

There is a wide variety of models and parameters extraction procedures to characterize the crosstalk between transmission lines [7, 9, 5]. A simple and efficient model is proposed by [1], which considers only the capacitance between the lumped lines, and represent it with grouped elements. A more complete analysis in which the magnetic coupling between the series inductors of the TL are modeled is presented in [7]. However, according to [1], the model accounting only the parasitic capacitance of the lines is satisfactory to describe this phenomenon in integrated circuits, given the short distance between the lines, their dimensions and the presence of an insulator around the whole structure, portraying a typical capacitive effect, much higher than the paths inductance.

## 3. PROPOSED ANALYSIS AND MODELING

In order to evaluate the crosstalk effect between two lines in an integrated circuit, several configurations of lines are proposed. These layouts were designed in a CMOS 130 nm process and submitted to an electromagnectic (EM) simulation in the software ADS by Keysight in frequencies between 1 GHz and 10 GHz with 50 Ω terminations. Instead of using an electrical model, an EM simulation finds an approximate solution to Maxwell's equations that satisfy the given boundary conditions. This provides more accurate results for the studied phenomena. The coupling effect can be characterized by the scattering parameter of forward gain ($S_{21}$), which represents the voltage gain between aggressor and victim lines.

Figure 1 shows the five layout configurations evaluated: parallel lines (a), parallel lines with ground strip (b), overlapping lines (c), overlapping lines with spacing (d) and overlapping lines with ground strip (e). The tests were made using the three top metal layers available in the technology, named MA, E1 and LY. In a first set of tests, the two subject lines were designed with same width W = 40 $\mu$m and length L = 500 $\mu$m. These dimensions and layers are chosen based on sizes commonly used in the output of power amplifiers circuits, as in [8], where a power sensor based on crosstalk effect is used. The distance between lines, when applied (as pictured in Figure 1), was changed from 10 $\mu$m up to 160 $\mu$m. Also, in dispositions (b) and (e) the effect of an intermediary line connected to ground (named ground strip) is examined. The distance between aggresor and victim to the ground strip (same for both lines) was change from 10 $\mu$m to 60 $\mu$m. According to [7], the insertion of such a line between aggressor and victim should reduce the coupling significantly. In these cases, in addition to the separation distance, the width of the strip (Ws) is changed (from 10 $\mu$m to 60 $\mu$m).

The parallel configuration presents a high coupling and it is very used in IC routing. This arrangement is further explored in a second set of tests in which other parameters were swept. These other simulations were realized for two parallel lines in the metal layer MA (the thickest, allowing more noticeable results). The size of the paths (width and length) and their shape were evaluated. First, keeping the width for both lines fixed (W =40 $\mu$m), the length of the victim line is changed from 100 $\mu$m to 750 $\mu$m for three different aggressor lengths. The analog test is performed for the width of the lines. Both lengths are kept equal to 500

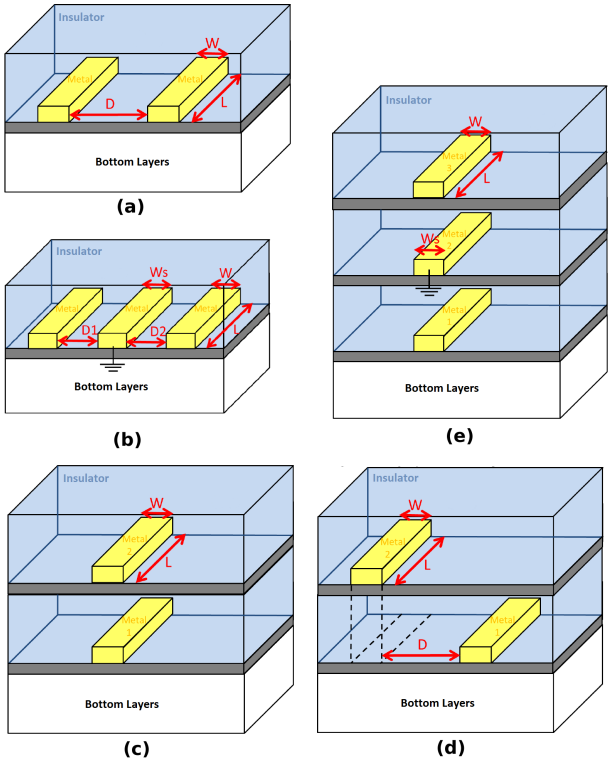


**Figure 1: Evaluated layout configurations and parameters**

$\mu$m and the victim width is changed from 10 $\mu$m to 80 $\mu$m for three different aggressor widths. Regarding the shapes, a straight aggressor line is considered, with a parallel victim line with a curve of 45 degrees or 90 degrees at only one point. The size of the lines is fixed and the parallel length is changed from 50 $\mu$m to 450 $\mu$m.

An electric model is considered to represent the behavior of the crosstalk effect between two lines. As described in Section 2, a grouped RC elements model is used. Figure 2 shows the equivalent circuit of the transmission lines. The values for the components are obtained from the results of EM simulation. The complex admittance parameters of the lines can be obtained direct from EM simulation. Considering that the components $R_1$, $R_2$, $C_1$ and $C_2$ represent the independent characteristics of each line, all coupling effect is represented by the capacitor $C_m$. Considering the admittance parameters, the values for these components can then be expressed as Equations 1 to 3:

$$R_1 = real\left(\frac{1}{Y_{33}}\right) \tag{1}$$

$$C_1 = \frac{imag(Y_{33})}{2 \cdot \pi \cdot f} \tag{2}$$

$$C_m = \frac{imag(Y_{34})}{2 \cdot \pi \cdot f} \tag{3}$$

where $f$ corresponds to the operation frequency and $Y_{ii}$ are the admittance parameters. The expression for $R_2$ and $C_2$

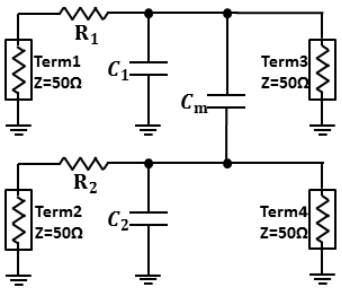


**Figure 2: Circuit modeling for the crosstalk effect.**

are similar to the ones for $R_1$ and $C_1$, but replacing the term $Y_{33}$ by $Y_{44}$. The capacitance $C_m$ is evaluated for performed parallel lines simulation.

# 4. SIMULATION RESULTS

The proposed layout configurations were submitted to electromagnetic simulation and the forward voltage gain ($S_{21}$) is considered at a frequency of 2.26 GHz for all evaluated configurations described in Section 3, as measure of the coupling effect.

Figure 3 shows the results for the different layout arrangements studied. For parallel lines (a), it is possible to notice the strong influence of separation distance between the lines and the similarity between the three different tested metal layers. The highest coupling simulated presents a $S_{21}$ of -27.1 dB and occurs for the metal layer MA with a separation distance of 10 $\mu$m. Only three scenarios are considered for overlapping lines configuration. The forward voltage gains are -18.3 dB for the layout using MA and E1 layers, -18.4 dB for E1 and LY layers and -22.7 dB for MA and LY respectively for aggressor and victim lines. These results indicate that a higher coupling (up to 8.8 dB difference for the same MA aggressor line) is achieved when using this strategy. This occurs because the oxide thickness between the metal layers is thinner than the smallest distance considered for the parallel lines. Considering the overlapping lines with spacing (results in Figure 3(b)), it can be noted that the coupling is very similar to the parallel lines (Figure 3(a)). This result indicates that the crosstalk effect is resultant of the interaction between the width of the paths. The electric field lines flow mainly from the top and bottom surfaces of the paths, which are larger than their thickness. These results support the modeling of the coupling as a capacitor between lines. Figure 3(c) shows the results for MA parallel lines with a ground strip in between, for several widths of the strip. Considering D = 10 $\mu$m and $W_s$ = 20$\mu$m, the total separation between these lines is 40 $\mu$m. Comparing the $S_{21}$ obtained with a strip line with the $S_{21}$ without it for this distance, one notices a 10.4 dB reduction. The strip insertion in overlapping lines results in reductions of $S_{21}$ from 8 dB (for $W_S$ = 40 $\mu$m) to 12.6 dB (for $W_S$ = 80 $\mu$m)

The principal results obtained for the parallel lines tests are depicted in Figure 4. Graph (a) shows the dependency of the crosstalk effect on length of victim line for several aggressor lengths. It shows that the longer one line is, the stronger is the dependency on the other line length. Graph (b) shows

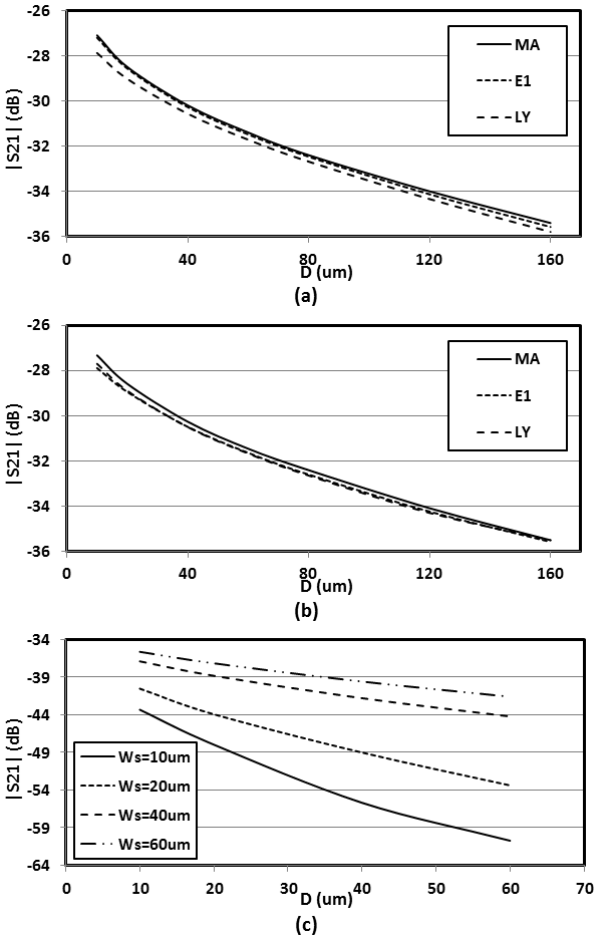


**Figure 3: EM Simulation Results for (a) parallel lines, (b) overlapping lines with spacing and (c) parallel lines with strip.**

the dependency on the width of the victim line for several aggressor widths. The influence of both length and width on $S_{21}$ do not depend on whether the victim or aggressor is changed. The resulting $S_{21}$ presents the same value for a determined change in either one of the lines. Graph (c) pictures the coupling dependency on the parallel length. It shows the dependency of the crosstalk effect on the total proximity of the paths.

The validation of the approximation by the electrical model and the values for the components is made by comparison between electrical and EM simulations. The results for $S_{21}$ obtained for both are showed in Figure 5 (a) and (b). Figure 5(a) corresponds to simple parallel lines configuration and Figure 5(b) to parallel lines with a 45° curve with parallel length of 200 $\mu$m. At the operation frequency of 2.26 GHz (frequency used for the parameter calculation), for parallel lines, electrical simulation gives a $S_{21}$ of -30.34 dB, while $S_{21}$ for EM simulation is -30.21 dB. This represents a 0.4% difference between the two methods. For the curved lines, the percentual difference is 1.5 %. Figure 5(c) shows the dependency of the capacitance $C_m$ on the distance between the lines, which has the same behavior as the $S_{21}$ parameter.

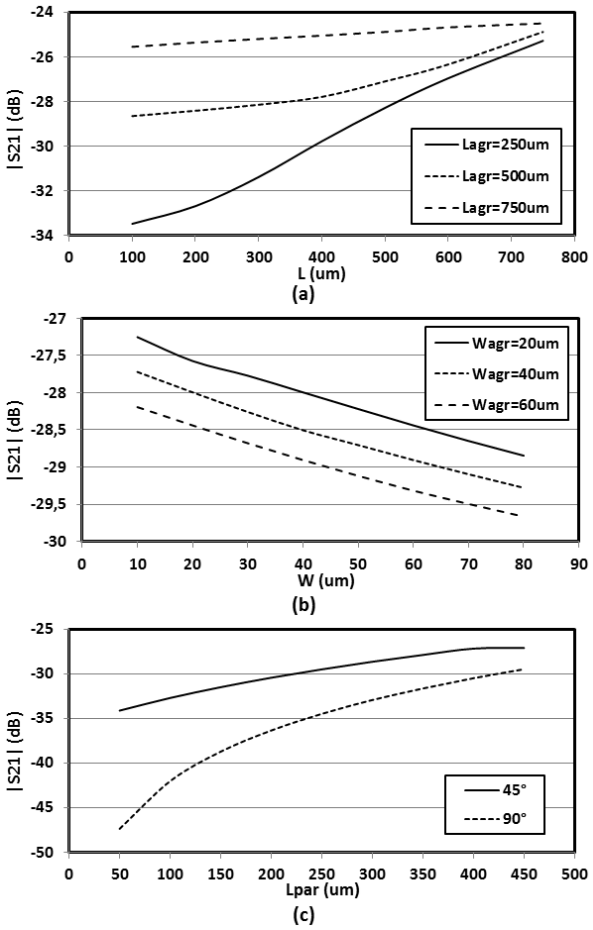


**Figure 4: EM Simulation Results for parallel lines, with variation of (a) length, (b) width and (c) parallel length.**

## 5. CONCLUSIONS

The analysis of parameters that influence crosstalk effect in integrated circuits and an electrical model for this effect were presented. Basic concepts about coupling effects between near lines in an integrated circuit were introduced and then applied to the specific study case. An electric model was presented, as well an estimate of component values based on electromagnetic simulation. A set of layout configurations was proposed in order to analyze and quantify this effect for different situations. This was performed through EM simulation of the lines for a 130 nm process. Results showed the behavior of the crosstalk effect (weighed by forward voltage gain - $S_{21}$ ) by means of layout variations. This parameter presented values between -62.4 dB and -18.3 dB for the considered tests. The electrical model was validated in comparison with the EM simulation, presented a maximal 1.5 % difference for the cases evaluated.

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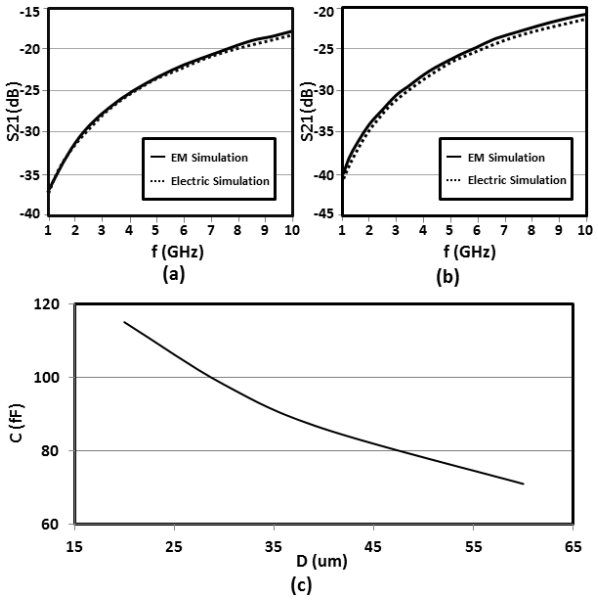


**Figure 5: (a)$S_{21}$ for parallel lines, (b) $S_{21}$ for parallel lines with 45° curve (c)$C_m$ as function of distance for parallel lines.**

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