Environmental Variability Impact in FinFET Full-Adders

Pablo M. da Silva, Alexandra L. Zimpeck, Ygor Aguiar and Ricardo Reis
Instituto de Informática – PPGC/PGMicro, Universidade Federal do Rio Grande do Sul, Brasil
{pmsilva, alzimpeck, yqaguiar, reis}@inf.ufrgs.br

ABSTRACT

This work demonstrates the impact of individual voltage and temperature variability as well as the simultaneous variability of voltage and temperature. These variabilities are considered environmental factors. The LSTP model proved to be more robust than the HP model. The TFA circuits using the HP model presented the worst performances for the variabilities analyzed. The Mirror circuit was robust to environmental variability.

CCS Concepts

• Hardware → Robustness → Hardware reliability → Process, voltage, and temperature variations.

Keywords

FinFET technology, environmental variability, 1-bit full-adders, simultaneous variability.

1. INTRODUCTION

The technology scaling down brought many benefits to the integrated circuits. The higher density, low power consumption and greater performance through the increase of clock frequency are examples of improvements. However, the CMOS bulk technology has reached its limit, and it is not trivial to continue with the circuit design in advanced technology nodes sub-22nm [1, 2]. In this context, the FinFET technology is pointed as an excellent alternative to replace it because multi-gate devices improve the Short Channel Effects (SCE) and decrease the leakage current paths [3].

Unfortunately, multi-gate devices have a high sensibility to PVT (Process, Voltage, and Temperature) variability. The main challenge associated with them is the uncertainty of circuit operation. It may cause the deviation on performance, abnormal power consumption and greater susceptibility to faults [4]. A circuit suffers variations on the voltage supply and the temperature along your lifetime [5]. Ensure the correct circuit operation even in the presence of environmental variability is crucial in any digital design.

Full adders are the focus of several studies because all processing happens through the operations that are executed by Arithmetic Logic Units (ALU). Moreover, full adders are connected in a cascaded block in some applications demanding the guarantee of performance from the initial stage. In this way, this work investigates the impact of environmental variability in 1-bit full-adders using FinFET devices in a set of predictive technological nodes. Two different models are used: the High Performance (HP) and the Low Standby Power (LSTP). The effects of the voltage and the temperature variations are considered simultaneously.

2. 1-BIT FULL ADDERS TOPOLOGIES

Full adders have a critical impact on the performance of simple and complex systems. Therefore, the electrical characteristics investigation of them is crucial to understand the circuit behavior at different operation conditions.

There are several topologies that implement 1-bit full adder circuits with different arrangements [6, 7]. This work considers five main architectures presents in the literature: Mirror CMOS Full Adder (Mirror), Complementary Pass-Transistor Logic (CPL), Hybrid Full Adder (Hybrid), Transmission Gate Adder (TGA) and Transmission Function Adder (TFA).

The Mirror topology uses the complementary CMOS logic, which has transistor complementary networks, while the CPL, TFA and TGA topologies explore the concept of the pass-transistor logic (PTL). The Hybrid topology realizes a merge of the two logic families previously mentioned to optimize both the power consumption and the performance [6]. A more detailed study of the topology characteristics can be found in [8].

3. VARIABILITY ISSUES

The need to reduce the power consumption and increase the speed of the circuits makes it necessary to reduce the supply voltage and increase the operating frequency of the circuits respectively. The increase in frequency causes an increase in the temperature of the joints and the whole die [9]. These factors make chips more susceptible to voltage and temperature variations that occur during circuit operation. These changes are considered environmental factors and are dependent on the design of the integrated circuit [5]. In addition to the variations of voltage and temperature, there are the physical factors, which are variations in the geometric dimensions and the electrical parameters resulting from the manufacturing process.

Islam et al. [3] analyzed the PVT variability effects in full adders operating in the sub-threshold region. The FinFET and MOSFET results were compared for CPL, Hybrid, Mirror and TFA topologies using the Berkley predictive model (BPTM) at 32nm. Similar research was made by Tahrim et al. [10] at 16nm. Ames et al. evaluate different architectures of 1-bit full-adder considering the PVT variability only in MOSFETs at 32nm in

[11]. In [13] the effects of PVT variability in FinFET full adders at 16nm considering the individual deviations were analyzed.

To the best of our knowledge, there is a lack of data about the effects of simultaneous PVT variability in FinFET devices. Thus, this paper verifies the impact of supply voltage and temperature variations at the same time in a set of 1-bit full adders topologies. The results helps to identify relevant behavioral standards concerning PVT variations and full adders in digital designs.

4. METHODOLOGY

The experimental setup considers the 7nm, 14nm and 20nm technologies nodes from PTM-MG [13] for both HP and LSTP models. The reference values for theses technologies are shown in Table 1. About devices, shorted-gate (SG) FinFET transistor and the minimum transistor sizing where all transistor with the number of fins equal to one was adopted. The full adders were descript in SPICE language and were simulated through HSPICE simulator. All the topologies have the fan-in and the fan-out equal to two and four inverters, respectively, to allow more realistic behavior estimation.

Table 1. Nominal values of the technological nodes.

Parameter	Technology (nm)		
	20	14	7
Voltage Supply (V)	0.9	0.8	0.7
Temperature (ºC)	25	25	25
Gate Length (nm)	24	18	11
Fin Height (nm)	28	23	18
Fin Width (nm)	15	10	6.5

For the analysis of variability, simulations were made changing the temperature and the supply voltage simultaneously. The temperature was varied in a range between 25ºC and 150ºC, and the nominal supply voltage suffers deviations among ±10%. from nominal values for each technology. The metric adopted to compare the circuits was the Power-Delay Product (PDP) that considers the worst case of propagation delays and the total power consumption.

5. ENVIRONMENTAL VARIABILITY

Under nominal conditions the worst result was TFA and the best result was TGA, which can be seen in Table 2. The other three circuits present very similar results.

5.1 HP Model

The circuits most impacted by environmental variability were the TFA and the CPL. Figure 1 shows the TFA behavior at 20nm through a heat map in which the x-axis is the temperature, the y-axis is the supply voltage and the color represents the PDP value according to the color scale. Figure 2 shows the CPL behavior at the same technological node in another heat map. It is possible to notice that although they behave in a similar way, the TFA circuit presents a result about 50% worse.

Table 2. PDP [aJ] nominal values (Temperature = 25ºC and VDD = nominal supply voltage of each technology)

Full-Adder	# Transistors	HP			LSTP		
		7nm	14nm	20nm	7nm	14nm	20nm
CPL	32	59.3	134.6	758.5	74.4	128.5	444.8
Hybrid	26	59.0	134.9	744.9	71.6	125.1	433.9
Mirror	28	58.0	129.4	757.6	73.3	124.8	431.3
TFA	**16**	**74.3**	**170.6**	**1156.3**	**77.3**	**131.8**	**482.6**
TGA	*20*	*54.9*	*124.1*	*720.4*	*71.5*	*118.6*	*402.7*

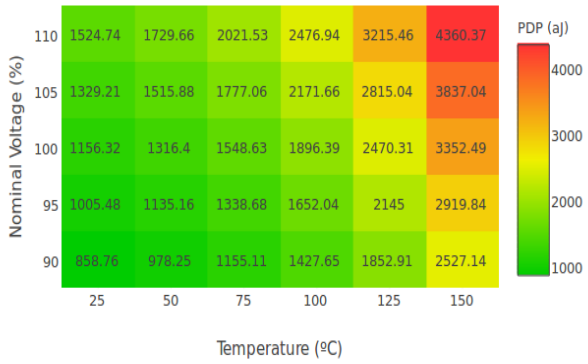

Figure 1. PDP heat map of TFA at 20nm.

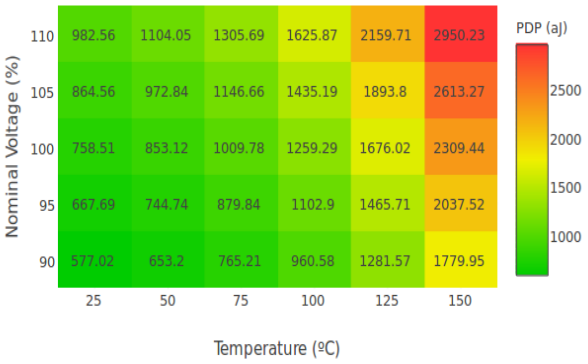

Figure 2. PDP heat map of CPL at 20nm.

Table 3 presents the minimum and the maximum PDP obtained in each circuit at each technology, in addition to the nominal values results (NV). It also displays the value relative to NV. The highest values were highlighted in bold and the smallest in bold and italic.

The minimum results obtained were at 25ºC and with the supply voltage -10%, while the maximum results were at 150ºC and the supply voltage 10% higher than the nominal value. These results showed that as the voltage and temperature increase the result of the circuits becomes worse. The temperature influences more on the circuit behavior than the voltage.

Table 3 shows that although the PDP of the circuits at 20nm is larger than in other technologies, the relative increase in the nominal values is greater in circuits at 7nm. So, the lower the technological node, the more susceptible to variations in supply voltage and temperature the circuits become. Δ represents how many times the PDP at 150 ° C is greater than the PDP at 25 ° C (nominal value). The TFA is highlighted in bold because it has the worst results.

Table 3. The impact of VT variability in FinFET full-adders using HP model.

Full-Adders		7nm			14nm		
		75ºC	**150ºC**	**Δ**	**75ºC**	**150ºC**	**Δ**
CPL	+10%	124.02	456.47	7,69	230.14	629.30	4,68
	-10%	78.98	292.45	4,93	144.08	401.54	2,98
Hybrid	+10%	119.95	418.45	7,09	223.99	586.68	4,35
	-10%	76.93	270.75	4,59	140.47	376.00	2,79
Mirror	+10%	118.96	421.86	7,27	221.97	585.86	4,53
	-10%	75.34	268.63	4,63	137.70	370.84	2,86
TFA	**+10%**	**160.07**	**579.98**	**7,81**	**302.29**	**811.93**	**4,76**
	-10%	**98.49**	**367.39**	**4,95**	**183.10**	**509.17**	**2,98**
TGA	+10%	113.13	410.77	7,49	211.61	575.56	4,64
	-10%	73.21	265.46	4,84	133.69	369.14	2,97

The PDP measures the average energy consumed per switching event, so the lower the PDP the better the circuit is. The best results were from the TGA circuit, but the Hybrid circuit presented a greater robustness to the VT variability considering the relative values Although there is an improvement of about 30% in the results at lower temperature and supply voltage, this effect is much lower than the increase in PDP caused by high voltage and temperature which can reach 681%.

Figure 3 shows the impact of VT variability on the TFA circuit at different technologies through a plot in which the x-axis is the temperature, the y-axis is the PDP and the traces correspond to a combination of the supply voltages and the technologies used. Similarly, figure 4 shows the behavior of the Hybrid circuit at different technologies.

5.2 LSTP Model

The TFA circuit is the most sensitive to simultaneous VT variations at 14nm and 20nm, but at 7nm the most sensitive was the Hybrid circuit. The best circuits was TFA, TGA, and Hybrid for 7nm, 14nm, and 20nm respectively. Figure 4 shows a comparison between TFA and Hybrid in several technological nodes through PDP absolute values.

Based on the results it was possible to note that the lower the voltage, the more temperature-sensitive the circuits become at 7nm. There should be a limit to the improvement of the results due to the increase in temperature because the TFA with supply voltage +10% has a worsening at 150ºC.

It can be clearly seen the difference between the HP and LSTP models through figure 5. It shows that while the HP model worsens with high voltages and temperatures, the LSTP model has an opposite behavior, obtaining a slight improvement with high voltages and temperatures. This behavior was observed in 7nm and 14nm technologies. The 20nm technology behaves similarly to the HP model, but with a much smaller variation.

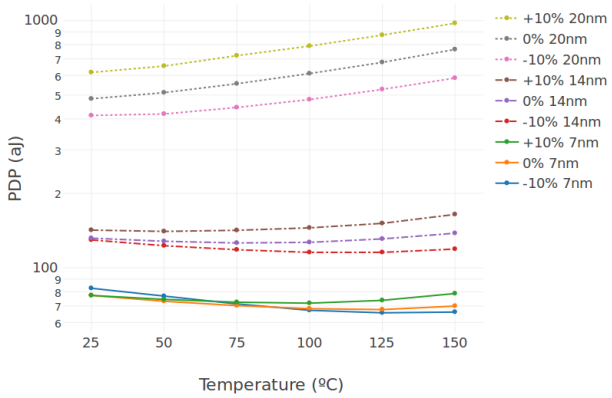

Figure 3. PDP impact of VT variability in TFA.

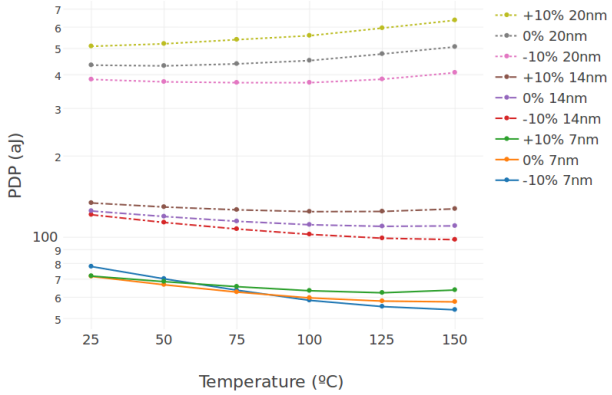

Figure 4. PDP impact of VT variability in Hybrid.

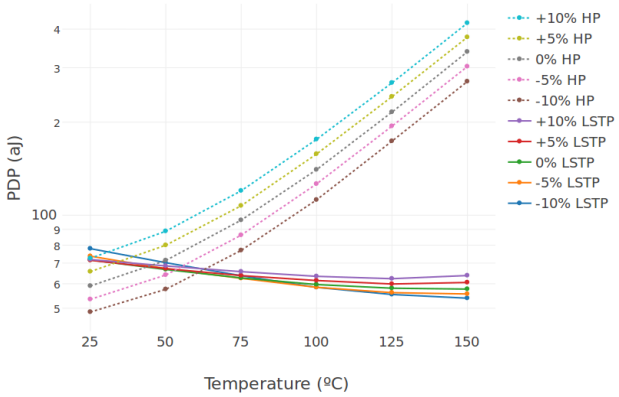

Figure 5. PDP difference of models in Hybrid at 7nm.

6. CONCLUSIONS

This work evaluates the impact of variations in supply voltage and temperature in 1-bit full-adders architectures using different FinFET technologies and models. Since the adders are the basis of simple controllers to the more complex processors, it is necessary to understand the behavior of these circuits when subjected to VT variability, to know which one is best-suited for certain circumstances.

The HP circuits suffer more the effects of supply voltage and temperature (VT) variability leading to a PDP increase of almost 8 times over the nominal value, while LSTP ones showed at most an increase of just over 2 times. Therefore it will be given greater prominence for circuits that use the HP model. Table 4 shows the best and the worst circuit considering Voltage (V), Temperature (T), and Voltage and Temperature simultaneously (VT).

Table 4. The Best and worst full adders in relation to individual and simultaneous environmental variations.

Variability	Best Case			Worst Case		
	Circuit	Tech (nm)	Model	Circuit	Tech (nm)	Model
V	Mirror	10	LSTP	TFA	20	HP
T	Mirror	16	LSTP	TFA	10	HP
VT	TFA	7	LSTP	TFA	10	HP

The most affected model was the HP. For the LSTP model, each technology has a different more robust circuit, while for the HP model the Hybrid is clearly the most robust. The TFA circuit besides having the worst PDP results, is also very sensitive to environmental variations in both HP and LSTP models, being the least robust in some technologies. The CPL and Hybrid circuits have also been shown to be sensitive to VT variability in HP and LSTP respectively. Future works will analyze the effects of process and voltage variability together, and the effects of temperature and process variability occurring concomitantly.

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