Analysis of basic parameters of proton irradiated n-channel FinFETs.

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***Abstract*—In this work, basic parameters extracted from the transfer curve of n-channel FinFET were evaluated before and after proton irradiation. This analysis was performed based on the drain current, the threshold voltage and subthreshold slope behaviors. In addition, the effects of back conduction on nFinFETs with wide fins were also evaluated. The results shows that large devices harshly suffers from radiation effects, but thinner devices barely show any change at all.**

Keywords—FinFETs, Proton radiation, Basic parameters

I. Introduction

The semiconductor industry aims to increase transistor density in integrated circuits for better performance and more efficiency in usage area. But, as far as MOSFET technology goes, diminishing the channel length may induce short channel effects (SCE) like threshold voltage roll-off, subthreshold slope degradation and gate current leakage, which degrades the overall performance of transistors.

To overcome such effects, Silicon-On-Insulator (SOI) MOSFETs were developed and these devices had reduced parasitic capacitance and increased current drive [1]. Even so, with continuous scaling down even this new technology starts to suffer with short channel effects. As a solution, multi-gate transistors like triple-gate FinFETs, shown in figure 1, were developed to increase the channel electrostatic control over the charges in the channel region [2], and to prevent the increasing of gate current leakage, high-k materials were used as gate oxide material.

In addition, with the evolution of technology, understanding the effect of radiation on the devices becomes of great importance since it starts to have several applications, as the proton therapy that is used in cancer treatment and satellites where radiation is inherent to its environment. In this paper, the effects of proton radiation in n-channel FinFETs with both large and thin fin width are investigated.

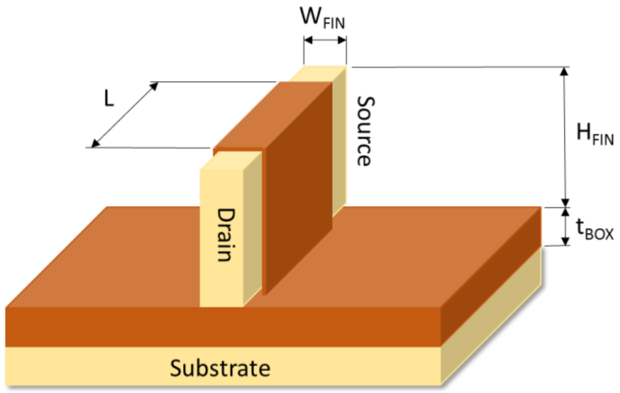

Fig. 1. Schematic FinFET structure.

II. Device Characteristics

The studied devices were nFinFETs, fabricated at Imec, Belgium, on a SOI substrate with 145 nm thickness of SiO_2 layer. The fin height (H_{Fin}) is 65 nm, the channel length (L) evaluated are 40 nm, 150 nm, 400 nm and 800 nm and fin width (W_{Fin}) of 20 nm and 870nm.

The devices are evaluated before and after proton radiation. The radiation was performed at the Cyclone facility in Louvain-la-Neuve (Belgium) with energy of 60 MeV and a fluence of 10^{12} p/cm^2 with no bias applied.

All devices have 5 fins in parallel and the source and drain contacts with selective epitaxial growth in order to minimize the series resistance

The measurements were made using the analyzer parameters B1500(Keysight).

A TEM image of measured devices is presented in figure 2.

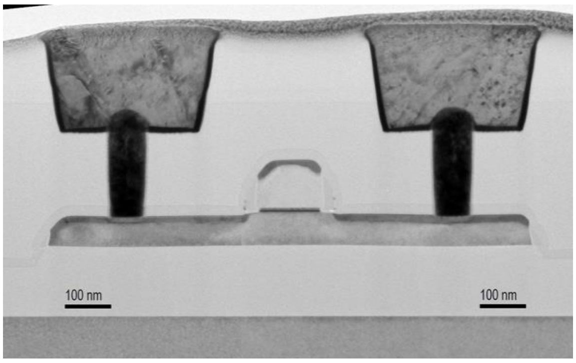

Fig. 2.TEM image of tri-gate FinFET crosssection.

III. RESULTS AND ANALYSIS

Figure 3 presents the drain current as a function of gate voltage for several channel lengths for narrow (A) and wide (B) devices. From figure 3A, it is possible to observe that the on-state drain current increases as the channel length decreases as expected, but when the subthreshold region is analyzed, a degradation of subthreshold slope (SS) as well as a shift of I_{DS} towards smaller V_{GS} occurs for the smallest channel length. Both the shift and a degradation in SS behavior suggests that this device is affected by SCE.3

In figure 3B the transfer characteristic is showed for W_{FIN}=870nm. The SCE for transistor with L=40nm is so strong that a very large leakage current does not allow to turn off the device for the studied gate voltage range. Although, in linear scale, it is not possible to observe any I_{DS} anomaly for devices with L>150nm, when the same curves are evaluated in log scale, a degradation of subthreshold slope (SS), for channel length 40nm and 150nm, can be observed, as well as, a shift of I_{DS} towards smaller V_{GS}. The shift of I_{DS} suggests a threshold voltage (V_{TH}) reduction caused by the SCE and a degradation in SS behavior is caused by the conduction of leakage current at back interface. Only the longest transistor apparently does not suffer from SCE.

Figure 4 shows the threshold voltage and subthreshold slope as a function of channel length. Analyzing its parameters for W_{FIN} = 20 nm, it is possible to notice that the SS value slightly increases only for a transistor with L=40nm and V_{TH} values are kept almost constant. It is worth pointing out that SS values are very close to the theoretical limit of MOSFETs devices.

However, for large W_{FIN}, threshold voltage for L = 40 nm was not possible to extract due to the high parasitic conduction, which would result in negative V_{TH}. Focusing on SS values it is possible to observe that the transistor with L=150 nm is already affected by short channel effect. Although it was not possible to extract V_{TH} and SS for large W_{FIN} with L=40nm, in figure 4 is shown its tendency in dashed lines, based on MOS technology typical behavior for short channel effects.

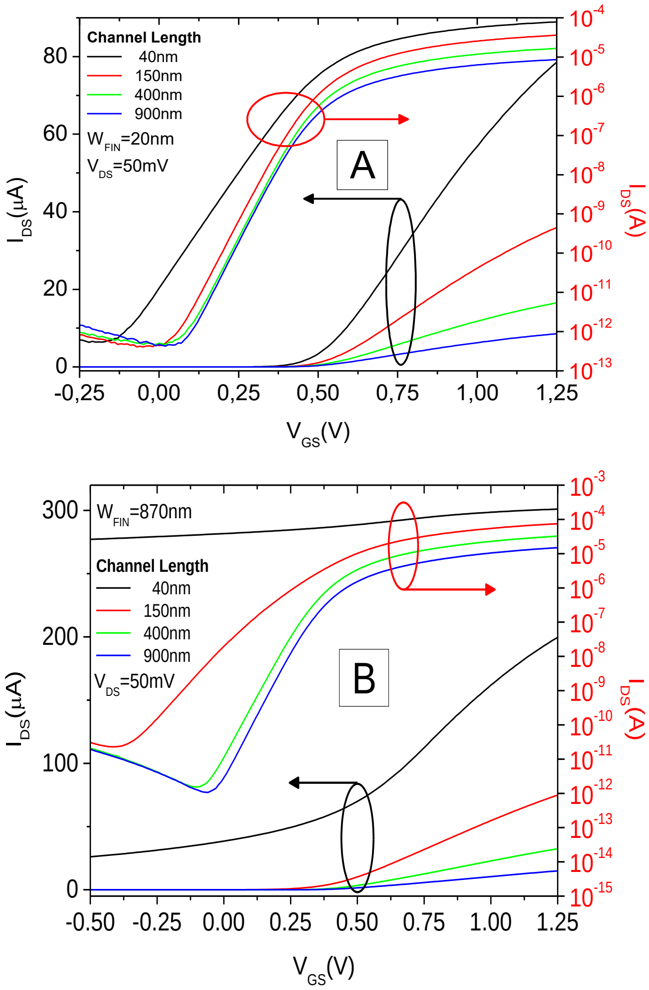

Fig. 3. Drain current as a function of gate voltage for FinFET with W_{FIN} = 20 nm(A) and W_{FIN} = 870 nm(B) for different channel length.

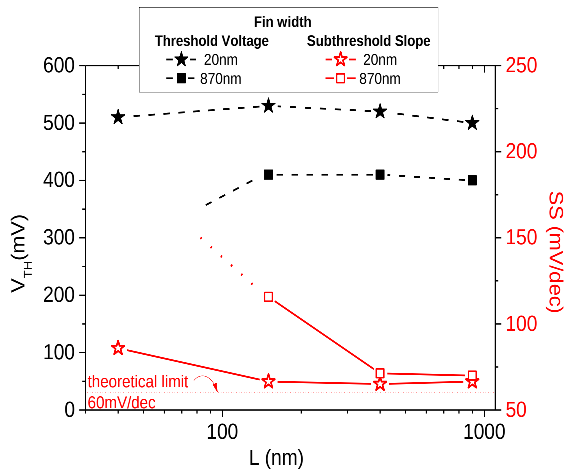

Fig. 4. Threshold voltage and subthreshold slope as a function of L for W_{FIN} = 20 nm and W_{FIN} = 870 nm.

Aiming to compensate the back interface conduction, in FinFETs with large W_{FIN} and short channel (40 nm), the back gate voltage (V_{GB}) can be set as a counterbalance. In figure 5, it is shown the transfer curve for different back gate voltage values.

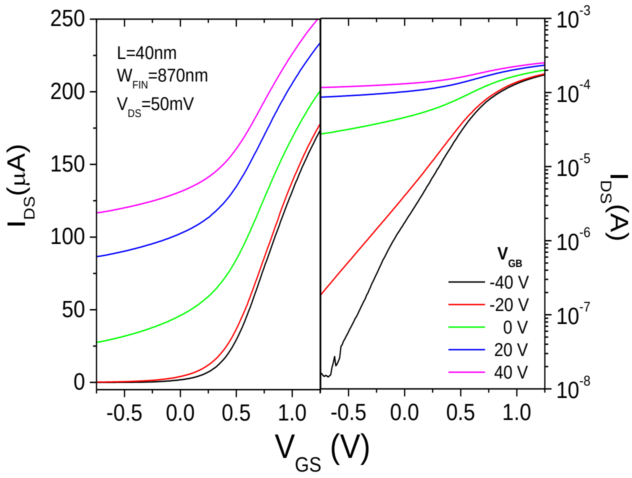

Fig. 5. Transfer curve of FinFET with W_{FIN} = 870 nm and L = 40 nm, for back gate voltage (V_{GB}) ranging from -40 V to 40 V with a step of 20 V.

For values above 0 V it is possible to observe that the parasitic conduction is worsened becoming even higher, but when negative values were applied, it tends to suppress the back conduction. It is possible to observe that for V_{GB}=-40V, the back conduction is almost nullified.

Since the nFinFET with L=40nm is affected by SCE even for the narrowest device (W_{FIN}=20nm) and the main effect of radiation in SOI technology occurs in buried oxide due to its thickness, the proton radiation influence on SOI FinFETs was evaluated for devices with L=150nm varying the channel width.

In figure 6, it is presented the transfer curve for pre and post radiation devices varying the channel width from 870nm down to 20nm. When the device with large W_{FIN} is irradiated with protons, the generated charges are trapped in the oxide, making the already existent parasitic conduction even stronger and consequently degrading the SS values. The effective V_{TH} is also shifted.

On the other hand, the radiation does not affect narrow FinFETs because the amount of generated charges that influences the back channel is insignificant compared to the greater electrostatic coupling created by the proximity of the side gates.

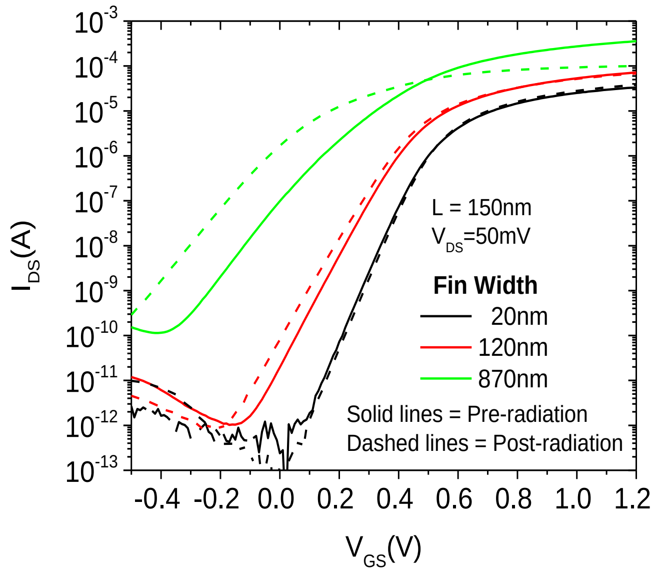

Fig. 6. Drain current as a function of gate voltage for different W_{FIN}.

Table 1 shows the values of V_{TH} and SS for different W_{FIN}, pre and post radiation. Focusing on SS values and knowing that radiation results in an increase of oxide and interface trap charges, since there is no significant variation on SS value for narrow devices, it is possible to conclude that the main reason to the SS degradation for wider fins is the parasitic back conduction. Analyzing V_{TH}, the trapped charges reduce the front and back threshold voltages, which results in a further reduction of V_{TH} as W_{FIN} increases.

TABLE I: Extracted threshold voltage (V_{TH}) and subthreshold slope (SS) for pre and post radiaton por Wfin = 20nm, 120 nm and 870 nm.

	Vth (V)		SS (mv/dec)	
	Pre-Radiation	Post-Radiation	Pre-Radiation	Post-Radiation
W_{FIN}=20nm	0.53	0.52	66	66
W_{FIN}=120nm	0.47	0.43	82	91
W_{FIN}=870nm	0.42	0.31	116	128

IV. Conclusions

Wider FinFETs have greater current drive than narrow ones, but its performance is worse due to the loss of the electrostatic coupling between the gate and channel. Even setting a very high V_{GB} to counterbalance the second interface conduction, it still occurs.

Narrow devices presents better performance when submitted to proton radiation, barely causing any effect at all. On the other hand, the performance of wide devices are harshly degraded by radiation. This degradation was observed because of the subthreshold slope increase and threshold voltage reduction.

Therefore, the narrowest nFinFET (W_{FIN}=20nm) present more immunity to radiation effects and better overall performance.

ACKNOWLEDGMENT

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