Fully Integrated Dual-mode RF CMOS Power Amplifier Design

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***Abstract*—Due to the low cost and high degree of integration of CMOS technology, mobile communication has widely spread around the globe. Most of the mobile devices are powered by batteries, which should be either charged or replaced at some point during its life. In this scenario, efficiency becomes a very important factor when designing these devices. In a radio transmitter, for instance, one of the largest power-consuming components is the power amplifier (PA). It is known that most PAs are generally sized to present their highest efficiency for high output power values, making it much less efficient when the output power needed is somewhat lower. Therefore, having two operating points that present good results for both scenarios turns out to be of great interest, as it greatly improves battery life. The circuit presented in this paper consists of two amplifying cells that when polarized accordingly, can provide two distinct operating modes, one of which is most effective for lower output power levels (back-off mode). The other one has better linearity and can reach higher output power levels, hence its designation (high power mode). Results prove that back-off mode is most effective when the signal's output power is close to 16 dBm, as PAE for this mode differs from high power mode in approximately 4.42 percentage points, but it is highly recommended to use it at output power levels anywhere from 5 to 21 dBm. Output power saturation occurs at around 25 dBm for high power mode and 22 dBm for back-off mode.**

***Index Terms*—power amplifier, radiofrequency, circuit design, CMOS, microelectronics**

I. Introduction

Radiofrequency power amplifiers (RFPAs) are employed in wireless communication systems and can often distort the signal and reduce the system's efficiency as a result of its non-linearity. Furthermore, power amplifiers are known for being one of the most power-consuming elements in radiofrequency frontends, which leads to impactful losses, whether it is because of the excessive heating of components or because of the power waste in the source. Provided that these systems operate on battery life, this becomes a topic of significant importance. [1]

When applying amplitude modulated signals to RFPAs, it becomes necessary for the designer to apply some techniques to improve its efficiency, as when varying the input signal's amplitude, there is an expressive increase in the system's overall loss. It is known that most PAs are generally sized to present their highest efficiency for high output power values, making it much less efficient when the output power needed is somewhat lower. Generally this is due to impedance mismatch, as it is almost always sized for a single input power value. [2]

Therefore, the main objective of this line of research is the optimization of power consumption and system efficiency.

A fully integrated, two-stage digitally programmable 130 nm CMOS power amplifier (PA) operating at 2.4 GHz was previously presented [3]. The lowest power mode achieves an 8.1 dBm saturation power and a 13.5 dB power gain.

A fully integrated CMOS power amplifier with discrete gain control for efficiency enhancement was previously presented [4]. The first of six stages is responsible for setting six gain levels controlled by a 3-bit cell, while the second stage provides power amplification. The association of these two stages allows reaching a gain from 22.4 dB to 31 dB.

In this paper, a dual-mode CMOS power amplifier that can operate efficiently at high power and power back-off is presented.

As follows, section II presents the circuit and the procedure executed in designing it. Section III evaluates the obtained results and shows comparisons between the two modes of operation. Finally, section IV concludes the discussion.

II. Circuit design

The purpose of this research is to design a dual-mode 2.4 GHz power amplifier using Globalfoundries 130 nm RF CMOS technology, i.e., to present a power amplifier with two distinct operation modes, one in which both PA cells are operating (best suited for higher output power values) and

another where only one of the cells is active (optimized for higher efficiency in back-off power values).

The circuit at hand is subdivided in three blocks, entitled "Power Splitter", "Power Amplifier A" and "Power Amplifier B", respectively. The objective is to split the power so that it can be made possible to have different operating points. To switch from one operating mode to another one of the bias voltages should be grounded. For high power operation, all bias voltages must be set according to table III. However, to operate in back-off mode the bias voltage of the common-gate transistor (V_{Bias2}) in "Power Amplifier A" should be set to zero (in section III the explanation for different configurations is elaborated). The equally split power will be combined after it passes through the power amplifiers, thus originating the main output. In Fig. 1 and Fig. 2 it is possible to observe the configuration more clearly.

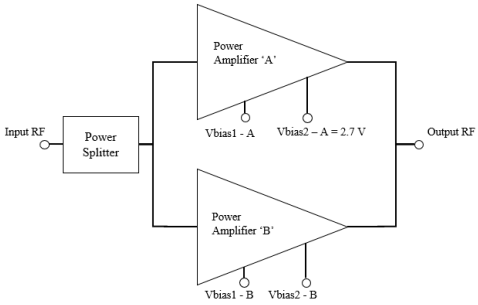

Fig. 1. RFPA High Power mode configuration - block diagram

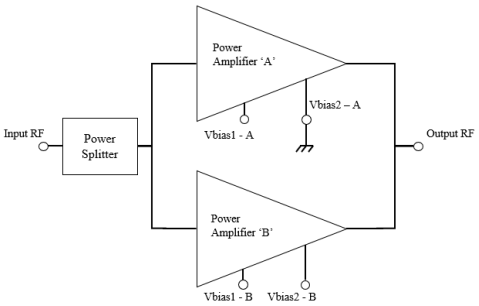

Fig. 2. RFPA Back-off mode configuration - block diagram

A. Power splitter

The splitter was designed using the Wilkinson topology, as depicted in Fig. 3. In order to obtain the capacitance and inductance values, simulations were made using Cadence Spectre RF varying both capacitance and inductance at the same time and trying to find the configuration that best fitted the objective, which is to have a transmission coefficient of -3 dB (equally split power). In Table I it is possible to observe the results for the passive components dimensions and parameters. Figures 4 and 5 represent the final simulation results for S parameters and phase shift for this block. It should be noted that in Fig. 4, the curves "Output 1" and "Output 2" are coincident, as well as curves "S22" and "S33". The same happens for curves "S21" and "S31" in Fig. 5.

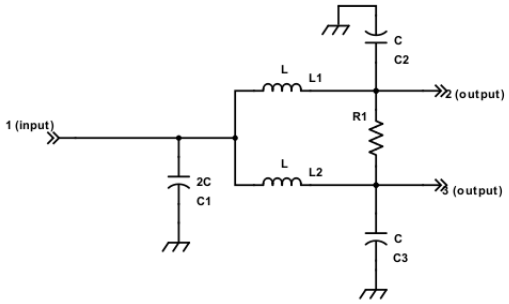

Fig. 3. Power splitter configuration - Wilkinson topology

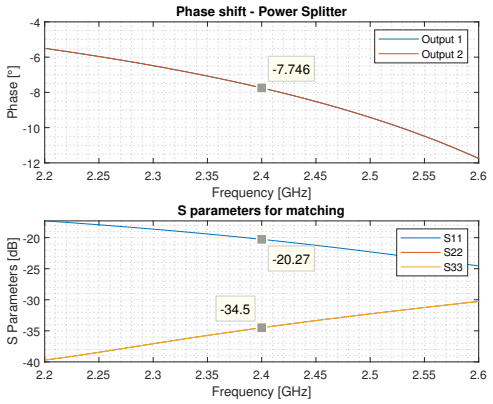

Fig. 4. Scattering parameters for matching and phase shift versus frequency (Marker at 2.4 GHz)

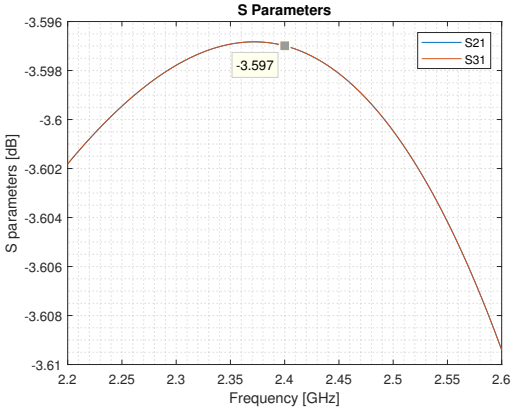

Fig. 5. Scattering parameters versus frequency (Marker at 2.4 GHz)

B. Power Amplifiers

The first PA (or "Power Amplifier A") is a cascode amplifier biased to class AB. The schematic used is depicted in Fig. 6

TABLE I
POWER SPLITTER PASSIVE COMPONENTS PARAMETERS

	Component parameters			
Component	**Value**	**Length/Outer Dimension (μm)**	**Width (μm)**	**No. of Turns**
C1	1.14 pF	20	56.56	-
C2	571.68 fF	20	27.28	-
C3	571.68 fF	20	27.28	-
L	4.45 nH	195,4	6	5
R	100.05Ω	9.36	5.92	-

and was also used for the configuration of "Power Amplifier B", with the exception of the bias voltage applied to the transistors. A thick oxide transistor was used for the common gate in order to withstand the output voltage swing, and thin oxide transistors were employed for the common source in order to enhance the gain. Simulations were made to size the passive and active components in order to achieve higher efficiency, gain and optimized input/output matching. The results for individual PAs can be verified in Fig. 7. Tables II and III contain the parameters used for both power amplifiers.

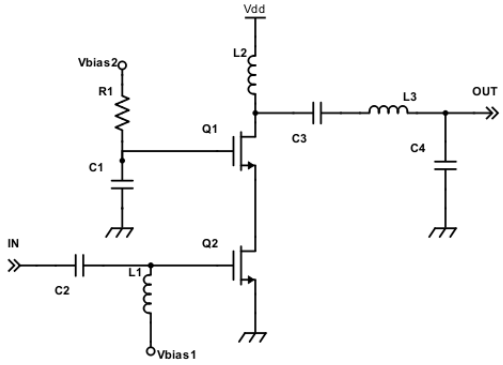

Fig. 6. Implemented cascode power amplifier configuration [5]

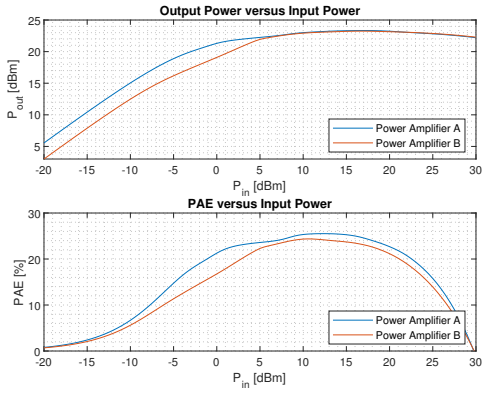

Fig. 7. P_{OUT} versus P_{IN} and PAE for both amplifiers

TABLE II
POWER AMPLIFIER PASSIVE COMPONENTS PARAMETERS

	Component Parameters			
Component	**Value**	**Length/Outer Dimension (μm)**	**Width (μm)**	**No. of Turns**
C1	1.96 pF	25	77.87	-
C2	1.96 pF	25	77.87	-
C3	8.8 pF	92	95.4	-
C4	916.98 fF	25	36.37	-
R1	999.96Ω	101.88	5.92	-
L1	572 pH	128.86	10	2
L2	900 pH	166.54	10	2
L3	2.22 nH	210	10	3

TABLE III
POWER AMPLIFIER ACTIVE COMPONENTS PARAMETERS AND BIAS VOLTAGES

	Component		Amplifier	
Parameters	**Q1**	**Q2**	**PA A**	**PA B**
Width (m)	2.28 m	1.12 m	-	-
Length (m)	240 n	120 n	-	-
No. of Fingers	114	56	-	-
Multiplicity	2	2	-	-
Vbias1	-	-	525 mV	450 mV
Vbias2	-	-	2.7 V	3.3 V
VDD	-	-	3.3 V	3.3 V

III. RESULTS AND DISCUSSION

After placing the designed blocks according to figures 1 and 2, the design is complete. Hereinafter, the results of the harmonic balance simulations (such as Gain versus P_{OUT}, PAE versus P_{OUT}, compression points), scattering parameters simulations and operating modes shall be discussed.

As mentioned, there are two operating modes, high power and back-off modes. To switch from one to another is as simple as grounding one of the bias voltages. For high power operation, all bias voltages must be set according to table III. However, to operate in back-off mode the bias voltage of the common-gate transistor (V_{Bias2}) in "Power Amplifier A" should be set to zero. This procedure is executed to deactivate "Power Amplifier A" and only use "Power Amplifier B" when the output power required is lower.

Simulation results for both operating modes are depicted comparatively, so that it is possible to analize the results more easily. Figures 8, 9 and 10 depict the behavior of each operating mode for power gain, PAE and scattering parameters, respectively.

The interesting aspect of back-off mode is that it has a significantly better efficiency for slightly lower output power values (up to around 21 dBm).

On the other hand, compression points indicate that the latter has a broader range of linear operation, as OCP1 values for high power and back-off modes are 19.37 dBm and 12.74 dBm, respectively.

Another important factor to be taken into consideration is the saturated power level, which reaches values close to 25 dBm for high power mode and around 22 dBm for back-off

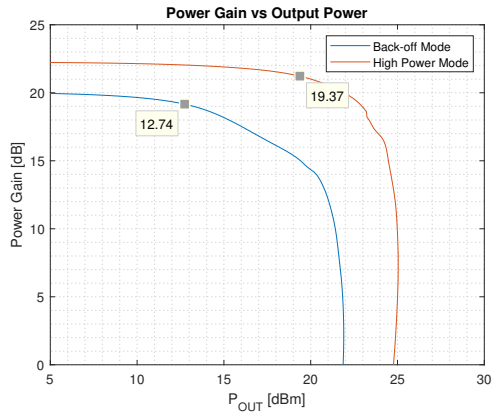

Fig. 8. Power Gain versus output power comparison (Markers show OCP1)

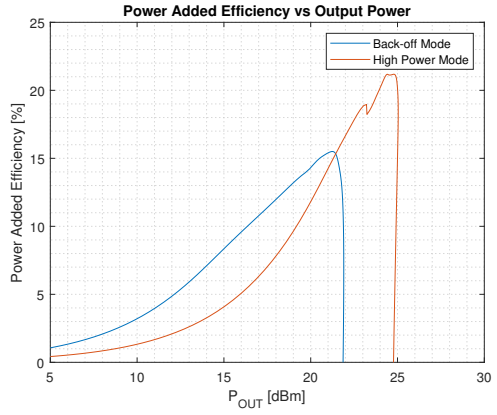

Fig. 9. Power added efficiency versus output power comparison

mode. Small-signal gain values for high power and back-off modes are 22.22 dB and 19.95 dB, respectively.

The power added efficiency peak values for high power mode is 21.18%, while back-off mode is considerably lower (15.5%).

Furthermore, it can be observed that in output power values around 16 dBm, back-off mode usage is optimally beneficial, as the PAE difference to high power mode is maximum at this point (approximately 4.42 p.p. higher).

Table IV summarizes these factors.

TABLE IV
MAIN SIMULATION RESULTS

	High Power Mode	Back-off Mode
OCP1 (dbm)	19.37	12.74
Saturation Power (dBm)	25	22
Peak PAE (%)	21.18	15.5
Small-signal gain (dB)	22.22	19.95
Recommended Output Power Range for usage (dBm)	>21	≤ 21

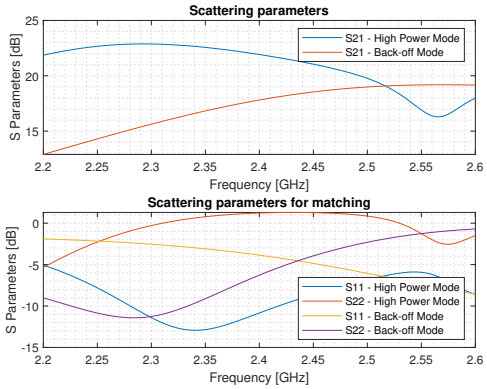

Fig. 10. Scattering parameters versus frequency comparison

IV. Conclusion

As power consumption of RF devices can sometimes be excessive, the main goal of this line of research is to maximize the efficiency in which power amplifiers operate on.

Dual-mode power amplifiers prove to be an effective solution to this problem, and this particular design has fulfilled its purpose.

The obtained results show that there are two distinct operating points that satisfy the purposes of this research, although impedance matching can be improved in future work.

In general, high power mode is more linear and reaches higher saturated power levels, while back-off mode dramatically increases efficiency for lower output power values. Results prove that back-off mode is most effective when the signal's output power is close to 16 dBm, as PAE for this mode differs from high power mode in approximately 4.42 p.p., nonetheless it is recommended to use it at output power levels anywhere from 5 to 21 dBm.

Small-signal gain is satisfactory for both operating modes, revolving around 19 dB and 22 dB for back-off and high power modes, respectively.

Furthermore, the increase in efficiency for lower output powers will prove useful in increasing the battery life of whatever device that applies this configuration.

References

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