Reducing variability impact on 7nm Mirror CMOS Layout

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***Abstract*— Process variability has been a critical challenge in emerging technologies because the circuits can deviate from their correct behavior affecting the manufacturing yield. New methods able to deal with the effects of process variability need to be investigated. In this way, this work analyzes the variability robustness using a technique based on the replacement of internal inverters by Schmitt Triggers in a traditional Mirror CMOS full adder. The full adder behavior was evaluated at nominal voltage conditions and operating at a near-threshold regime. Results show up to 11.39% and 21.84% improvement in average delay and energy variability robustness, respectively.**

Keywords—nanotechnology; process variability; full adder; schmitt trigger; ASAP7.

I. INTRODUCTION

During the last years, the integration capacity of digital circuits has increased significantly. This addition occurs due to the technology scaling allowing a larger number of transistors on a single chip. New challenges were introduced of integrated circuits design due scale down, as aging effects, leakage currents and increase in the number of faults [1].

Another undesired behavior verified in nanoscaled technologies is the process variability. Each circuit may present a different behavior due to variability during the manufacturing process. It can generate abnormal power consumption and deviation of performance, accelerating circuit degradation and making the circuit inappropriate for its initial purpose [1,2].

FinFET technology arose from the industry need for further scaling with acceptable yield and metric improvements. FinFET introduces a 3D structure which rises above the substrate resembling a fin. It has shown superior attributes, especially in the areas of performance, leakage power, intra-die variability and low voltage regime [3].

One of the most present logic blocks in computer systems is the Adder. It plays a central role in performing general arithmetic operations such as addition, subtraction, division and so on. Employed in the integer and floating-point arithmetic logic and memory address generation units, it defines the throughput being part of the critical path of electronic systems. Thus, any improvements over adding blocks generate a considerable gain in the whole system due to the huge influence of power, timing and area characteristics on the system design [4].

Schmitt triggers are commonly used as internal circuits on systems to provide enhanced noise tolerance and robustness against random variations in the input waveforms. In this way, Dokania et al. have proposed the application of Schmitt Trigger (ST) inverters technique into near-threshold Full Adder (FA) architectures to deal with process variability at transistor level design [5]. Their results show a significant reduction in timing and power deviation at 16nm bulk CMOS low power technology considering only the Carry Out output of the FA. Moreover, many works evaluate the effects of process, voltage and temperature (PVT) variability on circuits and devices [5-10], but there is a lack of techniques to mitigate the variability effects at the electrical or layout level.

Previous works do not evaluate the impact of the ST technique on layout level as well as in the FinFET technology. Therefore, this work evaluates an improvement of robustness over variability effects using a technique based on the replacement of traditional inverters by Schmitt Triggers on a Mirror CMOS full adder. The full adder behavior was investigated at nominal voltage conditions and operating at a near-threshold regime. The analysis has been performed at layout level using the 7nm FinFET technology node from ASAP7 [11].

This work is organized as follows: Section II introduces more in-depth information about variability and FinFET technology. Section III shows the methodology of this work. Section IV presents the results and discussions about them. Finally, Section V aims to conclude this work with final remarks.

II. VARIABILITY ISSUES

Standard CMOS devices have been optimized for high-speed and low-power consumption through its lifetime being the backbone of almost all modern digital circuits. The periodic process of technology scaling has resulted in faster and more energy efficient transistor than the previous generation. As channel lengths shrank below 50nm, the ratio of device size to atom-size becomes smaller, hence, a variable structure at the atomic scale has an increased effect on device behavior. However, the intrinsic quantum-mechanical limitations cannot be overcome, with their impact increasing as the technology shrinks further.

Variability consists of deviation of characteristics, internal or external, to the circuit. These characteristics or factors can be divided into three types. Temperature fluctuations and voltage drops cause environmental factors. Reliability factors are related to the aging process of the circuit. Physical factors are related to variations in geometrical and electrical

parameters caused mainly by the manufacturing process [2]. Fig. 1 shows the effects of physical variability on transistor structure. These effects are more prominent due to the technology scaling, and manufacturing tolerances are not correspondingly moving side by side.

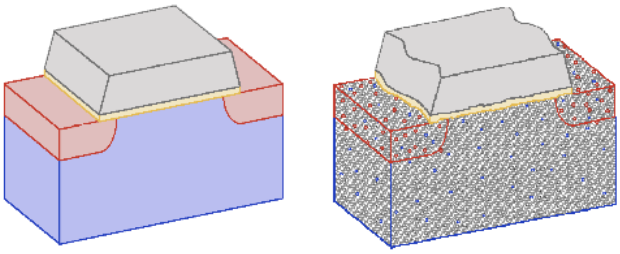

Fig. 1. Effects of physical variability on the transistor structure. Adapted from [12]

This work evaluated only the effects caused by the physical variability. Physical variations are responsible for deviations in the device work-function (WF), gate length (L_G), fin height (H_{FIN}), fin thickness (T_{SI}) and parasitic resistances. It is shown in [13] that work function fluctuation (WFF) is the leading cause of threshold voltage (V_{TH}) variations. Alongside, in [14] is shown the high correlation between the variability in I_{ON} and I_{OFF} currents and V_{TH} fluctuation in the presence of granularity of the metal gate. The primary cause of WFF is due to its dependency over the orientation of its metal grains. In the real fabrication process, metal gate devices are generally produced using multiple types of metal with different work functions randomly aligned. In the ideal fabrication process, metal gate devices have the gates manufactured with uniformly aligned metal and then, they have very low WFF deviation [15].

III. Methodology

For the experiments, it will be considered a Mirror CMOS Full Adder. Its robustness to process variability will be analyzed given that Schmitt Triggers will replace its internal inverters. The CMOS Full Adder has been chosen due to its promising results in related works [5,6]. The Full Adder schematic is shown in Fig. 2 with its internal inverters, which will be replaced by Schmitt Triggers highlighted in red.

The ST inverter schematic used in this work can be seen in Fig. 2, in the lower right corner. This circuit was based on [16] and modified in [5] to achieve the desired inverting characteristic. Their schematic consists of the junction of two inverters where the output from the second one will be the bulk for the first one. In this design, a dynamic body-bias technique is applied through a feedback mechanism to a standard CMOS inverter circuit allowing a change in the threshold voltage of two MOSFETs implying a change in the switching voltage. The ST also is designed to operate at a supply voltage equal to the 0.4V to achieve low power consumption.

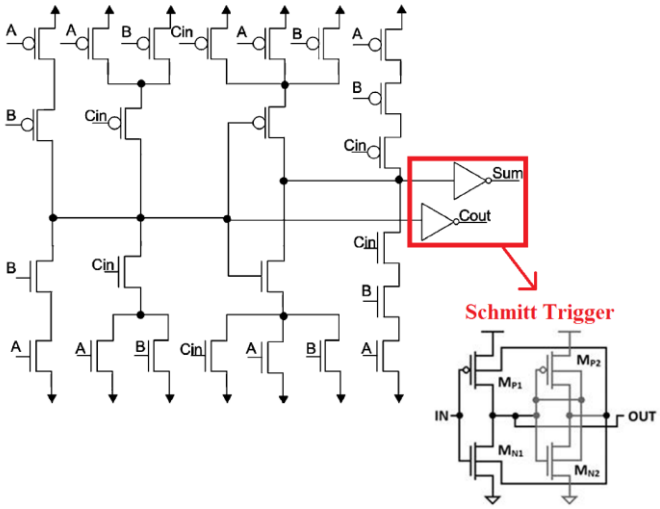

Fig. 2. Mirror CMOS full adder schematic with traditional inverters in red and the Schmitt Trigger schematic

Mirror CMOS Full Adder was designed using the Virtuoso Electronic Design Automation (EDA) tool from Cadence®. The Process Design Kit (PDK) adopted is the 7nm FinFET (ASAP7) from the Arizona State University in partnership with ARM [11]. For all layouts, it was used a dense 7.5 M2 (Metal 2) track cell baseline resulting in a 270nm cell height. The simulations were carried out in HSPICE from Synopsys, considering the new netlist obtained from the layout with the parasitic capacitances extraction. The full adder was designed with and without the Schmitt Triggers replacement to consider the penalties due to the adoption of the ST technique regarding area, power consumption and performance. For comparison, it was considered the simulations with nominal voltage (0.7V) and at near-threshold regime (0.4V). Table I summarizes the main devices parameters to electrical simulations and the widths/pitches of some key layers from ASAP7 technology.

Table I – ASAP7 device parameters and widths/pitches of some key layers [11]

Device Parameters	Nominal Supply Voltage		0.7 V
	Gate Length (L_G)		21nm
	Fin Width (W_{FIN})		6.5nm
	Fin Height (H_{FIN})		32nm
	Oxide Thickness (Tox)		2.1nm
	Channel Doping		$1x10^{22}$ m^{-3}
	Source/Drain Doping		$2x10^{26}$ m^{-3}
	Work-Function	NFET	4.3720
		PFET	4.8108
Layout Layers		**Width**	**Pitch**
	Fin	6.5nm	27nm
	Active	54nm	108nm
	Gate	21nm	54nm
	SDT/LISD	25nm	54nm
	LIG	16nm	54nm
	VIA0-3	18nm	25nm
	M1-3	18nm	36nm

The process variability evaluation was taken through 2000 Monte Carlo simulations varying the work-function fluctuation (WFF) of the PMOS and NMOS devices according to a Gaussian distribution. It was considered a 3σ deviation and a 5% variation on nominal values. For all experiments, it will be observed maximum values, mean (μ), standard deviation (σ) and normalized standard deviation (σ/μ) for each metric: delay, power, and energy. The σ/μ relation represents the sensibility of the cell to process variability.

IV. Results

Table II and Table III show the process variability impact on propagation delay and energy consumption. The last column (Δ) represents the improvement of the design with ST considering the σ/μ relation compared with the traditional one. This parameter specifies how much better (positive values) or worst (negative values) is the impact of the addition of the ST technique comparing the normalized variability of the FAs without ST. The topologies operating at near-threshold voltage were labeled with NT.

TABLE II. PROCESS VARIABILITY IMPACT ON PROPAGATION TIME OF THE SUM AND CARRY OUT OUTPUTS AT NOMINAL AND NEAR-THRESHOLD VOLTAGES

Propagation Delay		*Max (ps)*	*μ (ps)*	*σ (ps)*	*σ/μ (%)*	*Δ (%)*
SUM	CMOS	90.47	15.76	3.54	22.47	3.64
	CMOS ST	111.19	21.25	4.58	21.56	
	CMOS NT	981.65	90.02	95.76	106.37	10.39
	CMOS ST NT	997.56	120.29	114.67	95.32	
C_{OUT}	CMOS	73.30	15.61	3.30	21.15	5.70
	CMOS ST	85.38	19.36	3.85	19.90	
	CMOS NT	980.24	102.07	119.79	117.36	11.39
	CMOS ST NT	976.18	119.02	123.90	104.10	

TABLE III. PROCESS VARIABILITY IMPACT ON ENERGY OF THE SUM AND CARRY OUT OUTPUTS AT NOMINAL AND NEAR-THRESHOLD VOLTAGES

Energy		*Max (fJ)*	*μ (fJ)*	*σ (fJ)*	*σ/μ (%)*	*Δ (%)*
SUM	CMOS	63.74	8.72	2.33	26.72	7.23
	CMOS ST	84.36	14.42	3.57	24.79	
	CMOS NT	42.71	4.29	1.84	43.00	20.71
	CMOS ST NT	56.58	7.29	2.49	34.10	
C_{OUT}	CMOS	72.97	12.56	3.24	25.78	21.84
	CMOS ST	98.33	19.86	4.00	20.15	
	CMOS NT	46.83	5.91	2.00	33.85	21.00
	CMOS ST NT	63.90	9.80	2.62	26.75	

The first evaluation compares the impact of process variability in the Mirror CMOS Full Adder at nominal voltage (0.7V). Table II show improvements in average delay robustness up to 3.64% (5.7%) on Sum (Carry Out) output. Table III shows an increase in energy robustness up to 7.23% (21.84%) on Sum (Carry Out) output. However, the ST replacement increased by 34.86% (24.06%) and 65.4% (58.08%) the average delay and energy for the Sum (Carry Out) output.

At near-threshold level (0.4V), according to Table II there is a considerable improvement on delay robustness up to 10.39% (11.39%) on Sum (Carry Out) output, being 2x (2.85x) higher than the results at nominal voltage. Energy measures presented similar results considering the Sum output with a 20.71% improvement, 2.86x higher. The Carry Out output was an exception with similar improvements at nominal and near-threshold regimes. These results show a better utilization of the Schmitt Trigger characteristics in a much more variability vulnerable environment due to the subthreshold operation when signals are not as stable. A summary of these improvements is shown in Fig. 3.

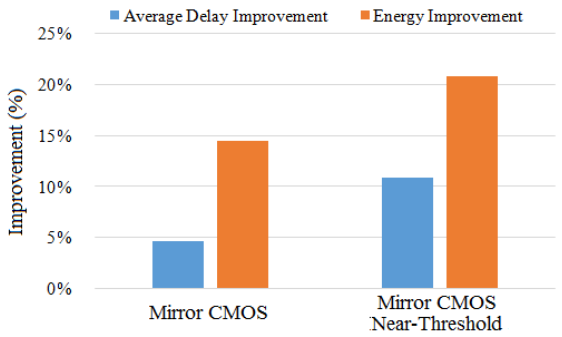

Fig. 3 Technique improvement comparison between nominal and near-threshold regimes

The ST replacement increased by 33.63% (16.61%) and 70.06% (65.76%) the average delay and energy for the Sum (Carry Out) output. It means that, at near-threshold level, the ST technique brings less performance and more energy penalty. This can be explained due to the increase in delays when the internal nodes, inputs, and outputs are charging/discharging leaving the path to the supply/ground closed increasing dynamic energy consumption.

The delay impact of the near-threshold operation regime is considerable. With an average 6x increase in propagation time and 49% average decrease in energy consumption, considering absolute values, in comparison to its version at nominal supply voltage. Consequently, there is an increase in standard deviation and normalized deviation absolute values with a 27x (36.29x) and 4.77x (5.62x) increase comparing the measures without the ST technique and a 25x (32.15x) and 4.44x (5.29x) increase considering the ST version for the Sum (Carry Out) outputs in comparison to their version at nominal supply operation.

This demonstrates the presence of considerable delay related deviation due to the near-threshold regime bringing inconsistency on the behavior of the circuit and higher charging/discharging times worsening the circuit performance, showing the need to find a sweet-spot for near-threshold operation supply voltage in order to get lower delay penalties and deviations maintaining the variability robustness increase and lower energy consumption.

A. *Penalties*

The increase in area is related to the technology rules from ASAP7. During the design process of the Schmitt Trigger, it was noted that it is not possible to connect the NMOS back-gate separately due to the shared substrate. The minimum well-to-well distance (equal to 108nm) and the necessity to apply TAP Cells to connect the back-gate terminal, increases the layout area considerably. Fig. 4 shows the traditional CMOS FA (an area equal to 340nm²) and the FA with the

Schmitt Trigger replacement applied (an area equal to 850nm²). The CMOS FA with ST technique had an increase in area of 150%.

The propagation delays and energy also are impacted due to the behavior of Schmitt Trigger. The ST needs to its input signal to reach a specific value for its charging or discharging to begin. Thus, such technique may show better results when applied to other technological nodes. Table IV summarizes the penalties, due to the technique, on average delay and energy regarding process variability robustness with the metrics increase for each output at both supply voltages.

TABLE IV. AVERAGE PENALTIES ON PROPAGATION TIME AND ENERGY ON BOTH OUTPUTS AT NOMINAL AND NEAR-THRESHOLD VOLTAGES

Penalties (%)	**Nominal**		**Near-Threshold**	
	Sum	*Carry Out*	*Sum*	*Carry Out*
Average Delay	34.86	24.06	33.63	16.61
Energy	65.4	58.08	70.06	65.76

V. FINAL REMARKS

This work investigates the replacement of traditional inverters on Mirror CMOS full adder by Schmitt Triggers. The full adder behavior was investigated at voltage nominal conditions and operating at a near-threshold regime. The obtained results comply with related works [5,10] and presents promising benefits regarding process variability mitigation. Results show an improvement of 11.39% and 21.84% in average delay and energy variability robustness, respectively.

However, this method introduces a significant increase in area and power consumption. The impact on propagation delays is softer. Thus, this technique should be applied to specific projects where process variability attenuation is a priority, and performance and energy efficiency can be placed in the background. As the process variability is more meaningful in FinFET technologies, it is necessary to investigate others techniques able to decrease their impact on circuits.

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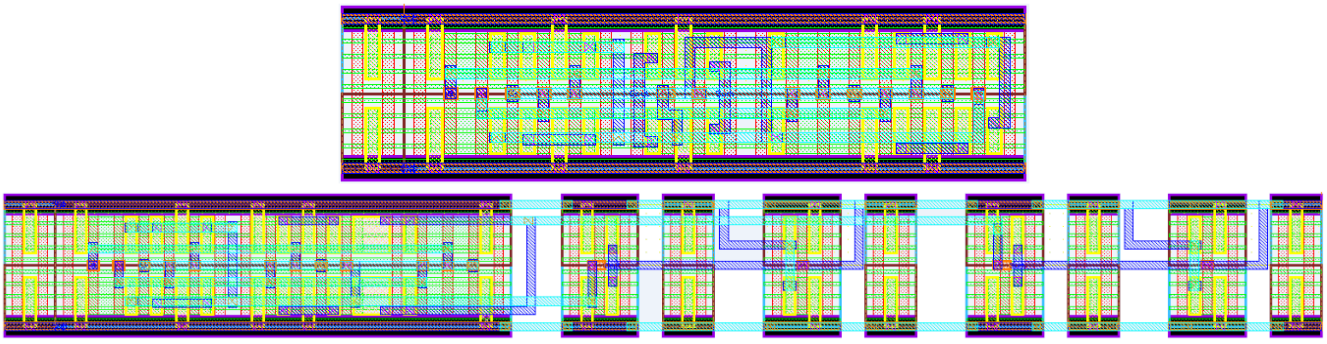

Fig. 4 Traditional CMOS Full Adder Layout (above) and the CMOS Full Adder Layout with the Schmitt Trigger replacement applied (below).