Digitally Controlled Current Driver Dedicated to Reconfigurable Power Amplifiers

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***Abstract*—This paper describes the design and application of a digitally controlled current driver for power supplying a voltage configurable power amplifier, implemented in 130 nm CMOS technology. Operating from 1.1 V to 1.8 V, the proposed circuit is an on-chip solution for switching the power supply of configurable power amplifiers in a completely digitally controlled way. This circuit can provide a maximum 230 mA current, for the highest power operation mode, only consuming 26.9 mW.**

I. Introduction

The world is getting more and more connected and the number of devices that are communicating with each other is increasing substantially. The projection for 2025 is that 75.44 billion devices are going to be connected [1], in a phenomenon called Internet of Things (IoT).

A great amount of these devices is mobile, which requires the use of batteries as power supply of those equipment. However, when using batteries, it is essential to take into account the lifetime of them. In order to extend the lifetime of the batteries, it is imperative to reduce the power consumption of these electronic devices.

One of the building-blocks that consumes the most energy in mobile devices is the power amplifier (PA) [2], which is responsible for the amplification of the radio frequency (RF) signal in RF transmitters. Traditionally, PAs are designed for the worst-case transmission scenario, when the output power in the transmitters is maximum. However, since this scenario occurs at specific moments in the devices operation, it is possible to optimize the energy consumption of such a PA through the reconfigurability of its supply voltage. This implies that when the PA does not require the maximum power at its output, its power supply voltage can be reduced, contributing to reduce power consumption of the overall transmission system.

To have this reconfigurability in supply voltage of the PA, it is necessary to design a circuit capable of feeding the current that the amplifier needs to operate, in addition to supplying the voltage of each stage. This paper presents the design of a digitally controlled current driver, that provides 1.1 V to 1.8 V voltages, with 100 mV steps, with a maximum current of 230 mA, implemented in 130 nm CMOS technology.

II. Reconfigurable PA Architecture

The focus of this paper is the application of the proposed current driver to PAs with reconfigurable supply voltage. The reconfigurable PA presented in [3] was used to validate the current driver proposed in this paper. The PA described in [3] has its output impedance and its supply voltage reconfigurable, working in different operation modes, defined by a 4 bits digital word that will change the operation mode according to the necessity of output power and impedance matching of the system. The reconfigurability aims to reduce power consumption of the amplifier, since each operation mode is designed to be the most efficient for a given operating condition.

This PA has its output impedance changed automatically with the operation mode switch, but its supply voltage has to be manually changed off-chip at the same time the digital signal switches the operation mode. Seeking for a fully integrated solution, this work provides an on-chip power supply reconfigurability. Figure 1 shows a block diagram of reconfigurable PA used, where the proposed current driver allows the power supply setup on chip using digital controlling words.

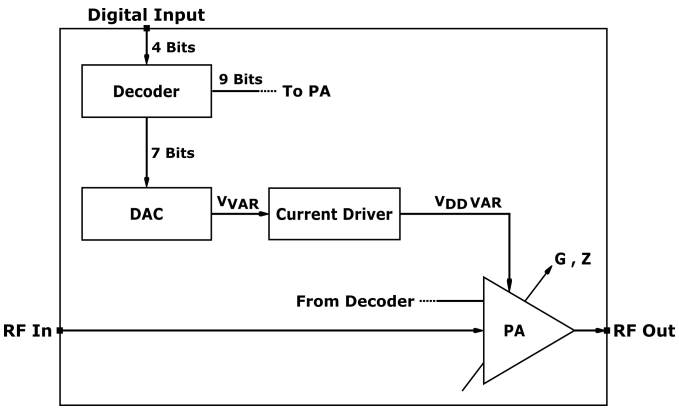

Fig. 1. Block Diagram of the circuit applied in a power amplifier.

The decoder integrated on-chip will receive the 4 bits digital word that defines the amplifier operation mode. The decoder provides a digital signal for the PA that will reconfigure the

output impedance, and another signal to the digital-to-analog converter (DAC), that will convert it to an analog voltage value, which will be the current driver input. The current driver will stably provide the supply voltage of the PA, with the capacity to deliver the required current for a given operation mode. That way, it is possible to configurate the supply voltage and the output impedance of the PA, in an automatic approach, controlled only by a digital signal.

III. Current Driver Circuit Design

The proposed current driver design is based on [4], consisting in two stages. The first stage is an operational amplifier that has the function to ensure a stable voltage to control the current driver output, guaranteeing the biasing of the power stage and blocking possible noises that will destabilize the output voltage. The second stage is the current driver itself, that will supply the necessary current that the PA needs to operate. All transistors were sized by the author, using Cadence Specter simulator to verify if they were working in the desired operating region.

A. Operational Amplifier

The operational amplifier depicted in figure 2 has a two-stage topology, using cascode current mirrors for self-biasing. The capacitor in the output assures a stable signal to control the next stage.

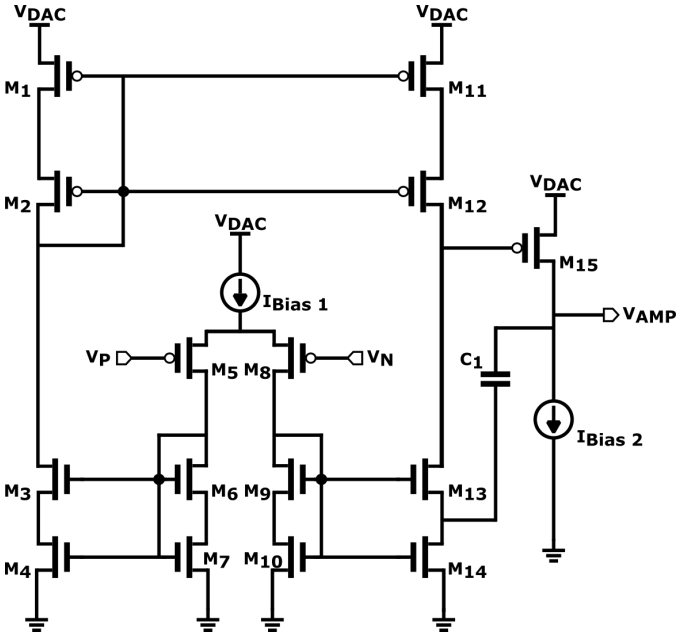

Fig. 2. Schematic of the operational amplifier.

M_1, M_2, M_{11}, M_{12}, M_3, M_4, M_6, M_7, M_9, M_{10}, M_{13} and M_{14} were sized for operating as cascodes current mirrors, which the transistors M_2, M_{12}, M_3, M_6, M_9 and M_{13} were dimensioned to operate in weak inversion, while M_1, M_{11}, M_4, M_7, M_{10} and M_{14} works in saturation.

This amplifier is a low consumption solution to ensure that transistor M_{20} has a stable voltage signal in its gate, since a slight variation in this voltage induces a considerable change in the circuit operation, resulting in a large drop of the V_{DD} value.

B. Current Driver

The current driver works based on a super source-follower configuration, set by transistors M_{18} and M_{19}, having the transistor M_{17} as a current source for the follower and M_{20} acting as a common gate amplifier [5]. This stage was designed to have a low output impedance, to avoid interference with the reconfigurable output impedance network. This circuit is composed by 22 parallel cells of this stage, in order to multiply the current, enough increasing it to suit PA demands. Figure 3 details the single cell's schematic.

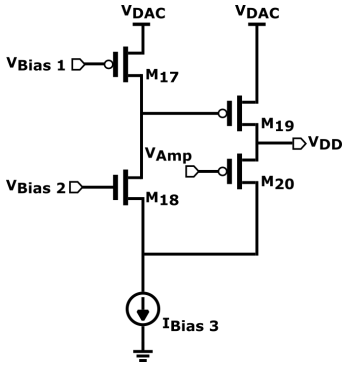

Fig. 3. Schematic of the current driver single stage.

The transistor M_{20} and M_{19} were designed to have a large channel width, thus being able to conduct a large current, but without leaving saturation region. The current source M_{17} was sized to have the drain current needed to bias the super source follower.

The driver was dimensioned to perform in the highest consumption condition, with a 1.8 V output voltage and 230 mA current, and then was adjusted to suit the other operation conditions.

C. Specifications

Table 1 presents all the operation modes implemented by the reference PA [3].

TABLE I
Output power of the PA for each operation mode

Operation Mode	V_{DD} (V)	I_{DC} (mA)	P_{DC} (mW)
1	1.8	230	414
2	1.8	188	338
3	1.8	157	283
4	1.7	159	270
5	1.8	133	240
6	1.6	135	216
7	1.5	136	204
8	1.5	119	178
9	1.6	100	160
10	1.4	96	134
11	1.2	99	119
12	1.1	101	111

V_{DD} value varies from 1.1 to 1.8 V, in 100 mV steps, having different power consumption for each mode. Note that the PA has a different power consumption for same V_{DD} modes. That occurs as a result of the other reconfigurabilities, such as variables output impedance and power gain stage. The other reconfigurabilities do not interfere in this application, since the function of this circuit is to provide supply voltage, delivering the required power, for each mode. In this way, the current driver was designed to suit this specification, being able to deliver the power required by the amplifier in each mode, operating in the correspondent voltage value.

IV. Simulations Results

The main goal of this study is to apply the designed circuit in power amplifiers. For this reason, simulations were performed in the schematic circuit described in [3], using Cadence Spectre simulator. For comparison purposes, the PA was both powered with an external power source feeding it and with the designed circuit as power supply. It is notable in table 2, that the circuit has a minor impact in the PA 1 dB compression point (OCP_{1dB}) and in the power gain (S_{21}), having a medium relative difference of 0.21 dB and 0.1 dB, respectively.

TABLE II
COMPARING THE PARAMETERS OCP_{1dB} AND S_{21} WITH AND WITHOUT THE DRIVER IN A FEW OPERATION MODES

Operation mode	With the driver		Without the driver	
	OCP_{1dB} (dBm)	S_{21} (dB)	OCP_{1dB} (dBm)	S_{21} (dB)
1	19.48	28.51	19.52	28.57
2	18.35	27.51	18.47	27.58
3	17.22	26.46	17.38	26.55
4	16.84	26.73	16.99	26.82
5	16.43	26.40	16.66	26.50
6	15.77	26.38	15.96	26.48
7	15.39	26.49	15.56	26.58
8	14.30	24.66	14.54	24.80
9	13.29	24.13	13.69	24.31
10	12.60	24.16	12.91	24.33
11	11.48	23.96	11.74	24.12
12	11.07	23.70	11.30	23.83

Table 3 presents the maximum values of the power-added efficiency (PAE) and the power consumption (P_{DC}) of the PA in both cases. It is possible to realize that the difference among values compared in this table is more significant in these parameters that was in the OCP_{1dB} and the S_{21}. P_{DC} has a medium relative difference of 3.95 % while PAE has a medium difference of 8.3 %.

It is easier to analyze this information by graphics, comparing each parameter of the PA with and without the current driver system. Looking at figure 4, one can note the small influence that the current driver circuit has in the OCP_{1dB}, having its highest relative difference of 0.4 dB at operation mode 9. Analyzing figure 5, it is notable that the driver barely affects the power gain, having a maximum difference of 0.18 dB.

TABLE III
COMPARING THE PARAMETERS PAE AND PDC WITH AND WITHOUT THE DRIVER IN A FEW OPERATION MODES

Operation mode	With the driver		Without the driver	
	PAE (%)	P_{DC} (mW)	PAE (%)	P_{DC} (mW)
1	23.96	441	25.8	414
2	22.62	356	24.47	338
3	20.89	296	22.58	283
4	20.01	282	21.7	270
5	20.34	249	22.31	240
6	19.33	225	21.03	216
7	18.61	213	20.21	204
8	16.83	185	18.45	178
9	15.71	153	17.81	160
10	14.75	138	16.39	134
11	12.79	123	14.05	119
12	12.47	115	13.63	111

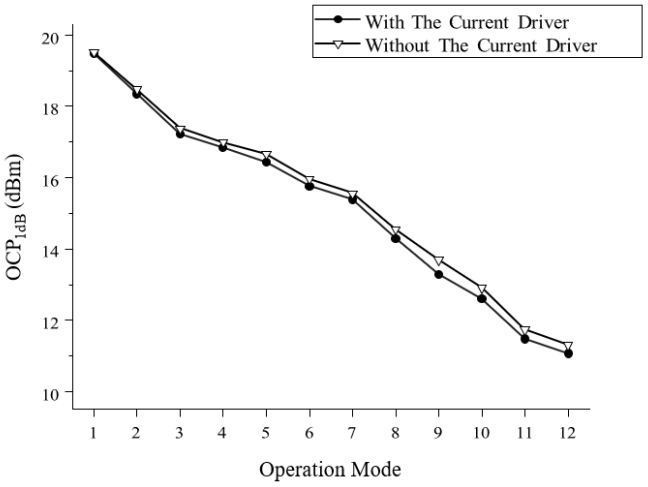

Fig. 4. OCP_{1dB} vs Operation mode, with and without the driver.

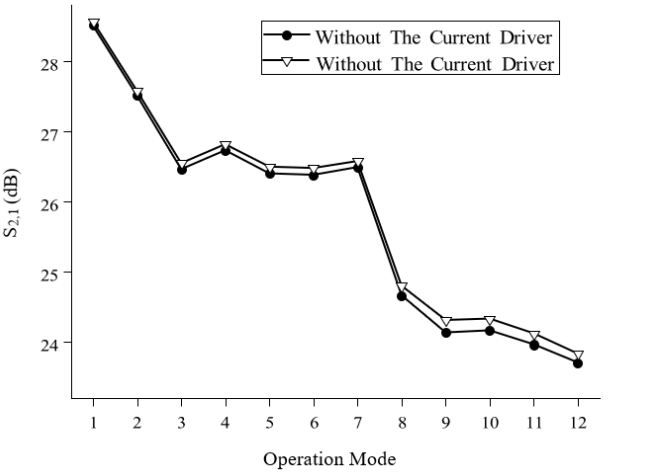

Fig. 5. S_{21} vs Operation mode, with and without the driver.

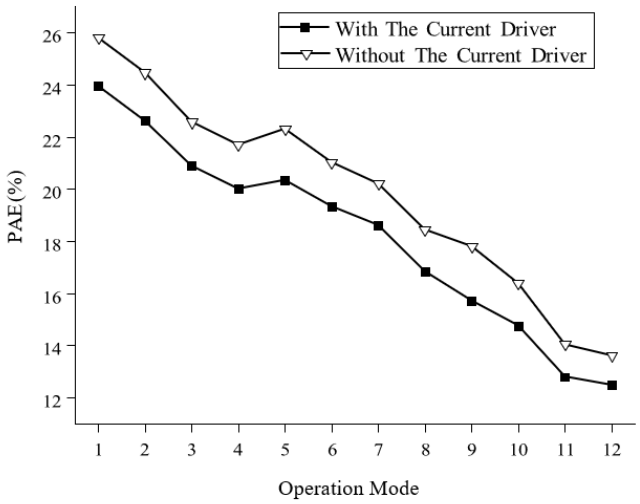

Fig. 6. PAE vs Operation mode, with and without the driver.

Now comparing power-added efficiency with and without the current driver, by looking at figure 6, it is possible to notice a higher difference among the values. This happens due to direct influence of the current driver in the overall system power consumption. In order to provide the current required by the PA, the current driver has a certain power consumption. A comparison of the PA power consumption with and without the current driver is depicted in figure 7. The highest relative difference in the PAE value is 11.79 %, occurring in operation mode 9. Even reducing the overall PAE, a circuit drive is not dispensable. The power consumption of the current driver is a price to pay to have a fully integrated solution of reconfigurable PAs.

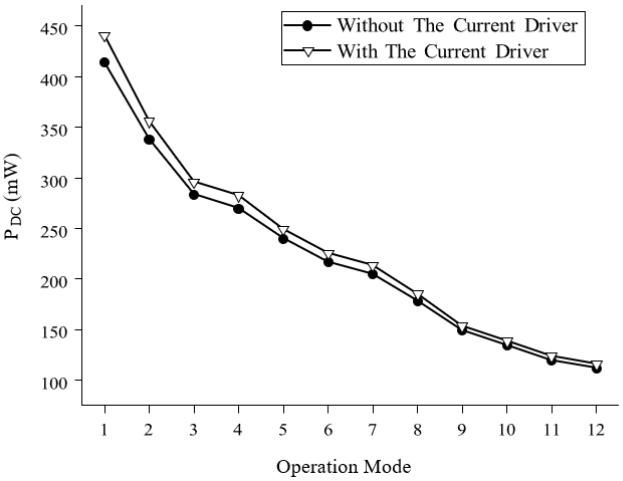

Fig. 7. P_{DC} vs Operation mode, with and without the driver.

From Figure 7, it is relevant to notice that for the lowest consumption modes, the difference between the traces decreases. This occurs because the current driver reduces its consumption as the current power demanded by the PA is smaller. It is also important to point out the small consumption of the driver, only 26.9 mW in the highest consumption mode, what represents a 6.5 % relative difference comparing to consumption without the driver.

V. Conclusion

This paper presents the design and discussion of a current driver system for power supplying a power amplifier with configurable voltage supply. The driver operates in a 1.1 V to 1.8 V range, with 100 mV steps, having a maximum current capacity of 230 mA. The circuit enables an on-chip solution for alternating supply voltage for PA digitally, consuming only 26.9 mW in the highest consumption mode and having a low intervention on the parameters of the amplifier, just a 0.18 dB difference in power gain, 0.4 dB in 1 dB compression point and 11.79 % in power-added efficiency, for the worst case.

References

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