Behavior of solar cells based on the OCTO MOSFETs

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Abstract— This paper proposes the implementation of solar cells layouted with the OCTO Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), which their gate geometries are octagonal. Several studies with solar cells implemented by using MOSFETs as a basic block have shown that is possible to improve the efficiency of the current solar cells. Thus, three dimensional numerical simulations will be performed in order to quantify the efficiency of these solar cells in comparison to the one implemented with a conventional way.

Keywords— Solar cells, MOSFETs, Unconventional gate Layout Styles for MOSFETs, OCTO MOSFET.

I. Introduction

The energy radiated by the Sun is greater than that consumed by humanity throughout its history and much greater than any other form of energy in the world. Figure 1 shows us an illustration of some energy potentials compared to the solar one [1].

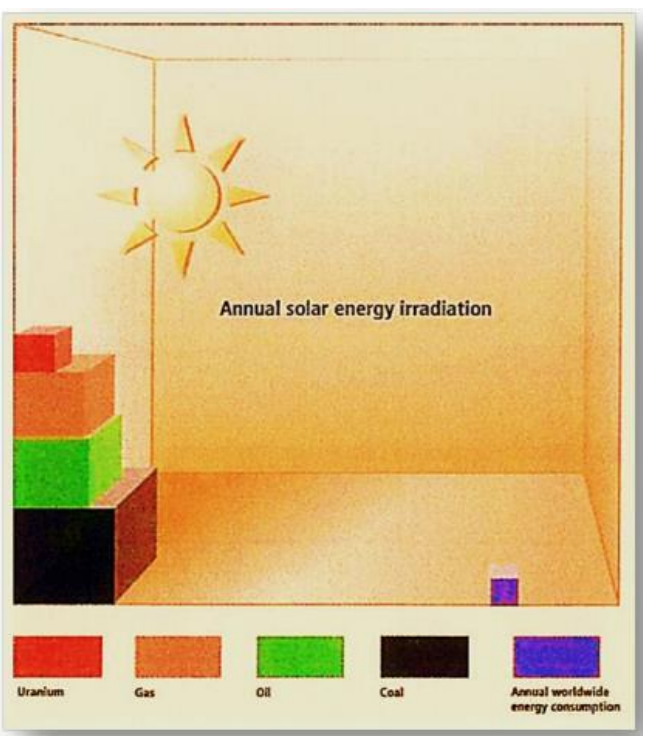

Figure 1: Comparison between solar energy and other forms of energy [1].

The great obstacle to the use of solar panels, is their low efficiency, resulting in increased cost of use with methods to supply it. Crystalline silicon solar panels are the most popular type. The great advantage of this type of solar panel, is the low cost of production and the ease of finding the raw material for silicon. It is estimated that the efficiency of the solar panels implemented with crystalline silicon is between 14% and 22% as shown in Figure 2 [2].

efficiency	percentage of total panels produced	in a simple way
>=18%	~ 10%	THE MOST EFFICIENT PANELS
17-17.9%	~ 30%	ABOVE AVERAGE EFFICIENCY
16-16.9%	~ 30%	EFFICIENCY OK
15-15.9%	~ 20%	BELOW AVERAGE EFFICIENCY
<15.0%	~ 10%	THE LESS EFFICIENT PANELS

Figure 2: Table with variation of efficiency of solar panels manufactured with crystalline technology [2].

The p-n junctions (diodes) are currently used to manufacture solar cells. But the use of MOSFETs to product them has already been studied as a better replacement for junctions [3].

In this scenario, to improve electrical performance of the solar cells, this paper aims to perform a preliminary study of solar cells implemented with biased Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) layouted with the OCTO layout style (octagonal door geometry, which it is capable of boost the electrical performance of the MOSFETs [4].

II. Literature review

A. Photoelectric effect

The photoelectric effect is when a material under radiation causes the electrons to be ejected as photoelectrons. The photons are particles that have an energy of their own. This energy (E) can be calculated using Equation (1) [1].

$$E = h * v \quad (1)$$

Where v is the photon frequency, where h is the plank constant. The photoelectric effect usually occurs on metal plates exposed to electromagnetic radiations [1].

B. Typical solar cell

The solar cell is responsible for putting into practice the laws of the photoelectric effect, that is, it performs the transformation of radiation into electrical energy [3].

When the solar cell does not receive any electromagnetic radiation, the only current that is generated is the diode current (I_D). Upon receiving electromagnetic radiation, the electric current called the photocurrent (I_{ph}) appears in the solar cell. The equivalent electrical circuit is illustrated in Figure 4 [3].

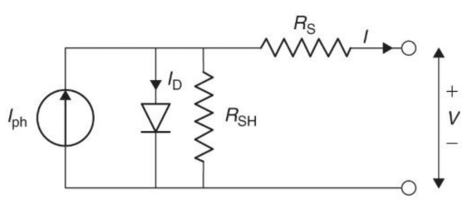

Figure 4: Electrical circuit equivalent of a solar cell [3].

In Figure 4, I_{ph} corresponds to the electric current generated, R_s corresponds to the internal resistance of the solar plate and R_{sh} refers to the shunt resistance. The V represents the output voltage directed to the load.

Figure 5 shows what a typical solar cell would look like [4].

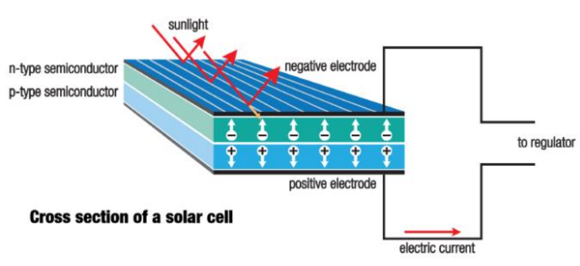

Figure 5: Cross-section of a typical solar cell [4].

C. Metal-Oxide-Semiconductor Field Effect Transistor

There are two different types of MOSFETs: channel p (pMOSFET) and channel n (nMOSFET). The n-type Metal-Oxide-Semiconductor Field-Effect-Transistor (nMOSFET). The n-type Metal-Oxide-Semiconductor Field-Effect-Transistor (nMOSFET) consists of a source and a drain, two highly conducting n-type semiconductor regions, which are isolated from the p-type substrate by reversed-biased p-n diodes. A metal or poly-crystalline gate covers the region between source and drain. The gate is separated from the semiconductor by the gate oxide. The basic structure of an n-type MOSFET is shown in Figure 6. The difference between the pMOSFET and nMOSFET is the doping. Usual MOSFETs have a rectangular gate geometry. This device has two modes of operation: enhancement and accumulation. In this paper, we are focusing on the enhancement mode [5].

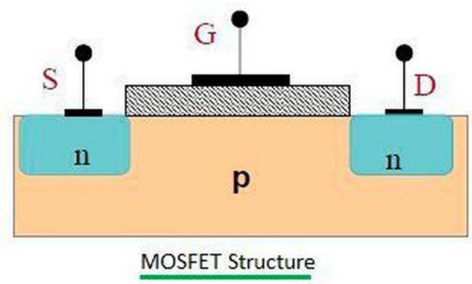

Figure 6: Structure of a conventional nMOSFET channel n [6].

For carriers moves happen, a voltage (V_{GS}) bigger than the threshold voltage (V_{TN}) must be applied between the gate and the source. So, a channel is created between the source and the drain that will make the passage of electrons occur. This current (I_D) have the longitudinal direction and can be controlled by the V_{GS} and $V_{DS.}$ Moreover, the current (I_D) is proportional to the ratio of the width (W) by the length (L) channel [6]. There are 3 modes of operation for MOSFET, the first is called the cut mode, which occurs when $V_{GS} < V_{TN}$ (where the current does not appear); the second is called triode mode, where it has a similar behavior to a resistor (V_{GS} higher or equal to Vt and V_{DS} smaller than $V_{GS} – V_{TN}$); the third is called saturation mode, which seems to behave as a current source (V_{GS} higher or equal to V_{TN} and V_{DS} higher or equal to $V_{GS} – V_{TN}$) [5].

Figure 7 shows the three operating modes and the current I_D behavior for different V_{GS} values of the nMOSFET [7].

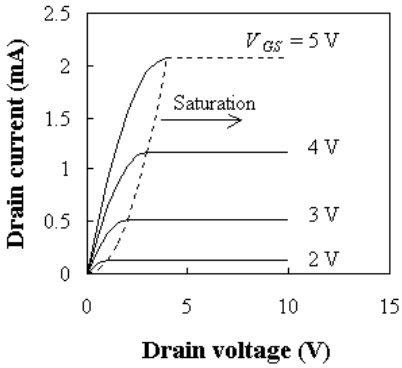

Figure 7: Characteristic curve Drain current curve (mA) vs Drain voltage (V) for different VGS values [7].

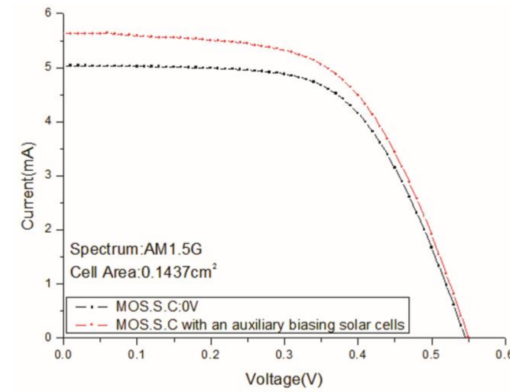

Figure 9: Photovoltaic I_{SC}-V_G characteristics of an MOS-structure solar cell measured under AM1.5G illumination and biased with an auxiliary source (Voc =5 V) [8]

D. MOS-structure solar cell

As shown in Figure 8 the MOS-structure solar cell consists of an n-type layer on a p-type silicon (Substrate), a thin gate oxide (SiO_2) layer, a transparent Tin Oxide Indian (ITO) gate electrode, two ohmic contacts on the drain and source regions, an electrode on the back (substrate) and an auxiliary voltage source, as shown in Figure 8 [8].

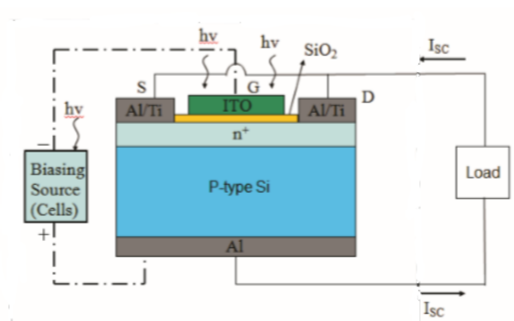

Figure 8: Cross-section of a MOS-Si photovoltaic cell with door polarization and the source and the drain in short [8].

With an external voltage source that is connected at its negative pole at the gate (ITO) and the positive at the substrate, it is possible to attract negative charges to the gate and thus reduce the depletion zone between n-type and p-type silicon. Thus, facilitating the flow of electrons from semiconductor n to semiconductor p. The source and drain contacts that are short-circuited and connected to a load that is connected to the substrate electrode, generate a current (I_{SC}), after the occurrence of electromagnetic radiation (figure 9). This current is generated because, when the electromagnetic radiation reaches the p-type material and the n-type material, the photoelectric effect occurs and thus, the electrons of the valence layer of the materials are released, generating the current through the source and drain (I_{SC}) [8].

Regarding a V_G of 5V, Figure 8 shows an increase of 12.93% in the I_{SC} in relation to the V_G is equal to 0V [8].

E. OCTO MOSFET

The OCTO MOSFET is a new layout style that emerged from the Diamond style (hexagonal gate shape) **[7-10].** When OCTO MOSFET is referenced, analyzes already done, guarantee us the advantages over traditional MOSFET in relation to the drain current (I_{DS}), IDS saturation (I_{DS_SAT}), transconductance (gm), maximum transconductance (gm_{-MAX}), gm / I_{DS} ratio , Early voltage (V_{EA}), intrinsic voltage gain (A_V), unit voltage gain frequency (f_T) and on-state drain / source series resistance (R_{ON}) [9] .

This innovative layout approach to manufacture MOSFETs adds new effects in the transistor structure that are able to significantly potentiate the electrical performance, such as the Longitudinal Corner Effect (LCE), the Parallel Association of MOSFETs with Different Channel Lengths Effect (PAMDLE) and to improve the radiation robustness regarding the Total Ionizing Dose (TID) effects, such as the DEactivate the Parasitic MOSFETs in the Birds Beak Regions Effect (DEPAMBBRE), without causing any extra cost for the current IC CMOS manufacturing process, because is simply a MOSFETs layout changing. The structure of OCTO SOI MOSFET (OSM) is shown in Figure 10 [9].

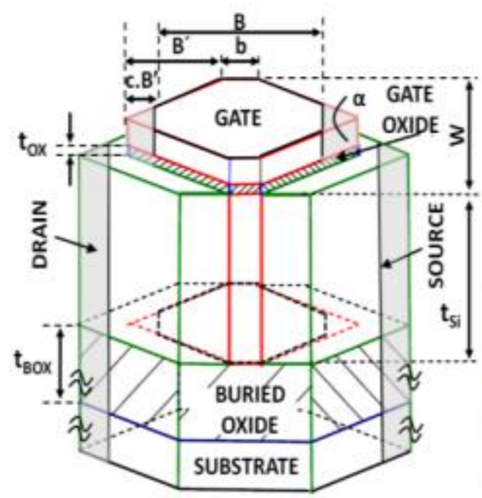

Figure 10: OCTO SOI MOSFET structure [9].

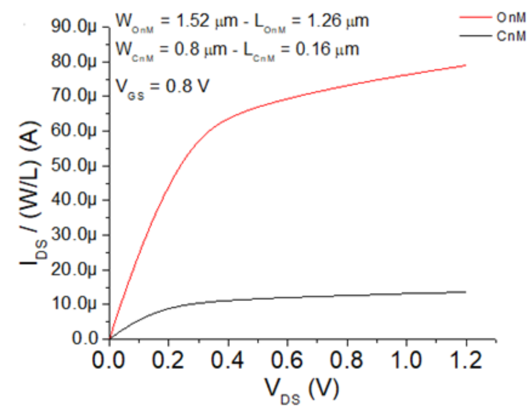

Figure 11: I_{DS}/(W/L) versus V_{DS} curves of CSM and OCTO, for V_{GS}=0.8V

In Figure 10, a, b and B are respectively the shorter and longer dimensions of the channel length (L), B is the height of the triangle part of the hexagonal gate geometry, c is the cut-factor, α is the angle formed by the triangle part edges of the hexagonal geometry of the Diamond, t_{ox}, t_{Si} and t_{BOX} are the gate oxide, silicon film and buried oxide thicknesses, respectively . The OSM effective channel length (L_{eff}), in first approximation, is given by (b+2B)/3 [10] .

The continuation of this work is to implement a new structure for the solar cell taking into account a base cell defined by the OCTO MOSFET that will be biased by using an external voltage source.

III. Experimental Results

To understand the behavior of the OCTO MOSFET (OnM), a comparison will be made in relation to the conventional MOSFET. For the analysis, Figure 10 was used, which shows how the flow current curves (I_{DS}) normalized by the aspect ratio [I_{DS} / (W / L)] as a function of V_{DS} for V_{GS} equal to 0.8V of an OCTO and the corresponding correspondent of the Conventional SOI MOSFET (CnM), with V_{TN}s (0.29 V) in both. Regarding that the two devices were submitted to the same bias conditions.

From figure 10, it is possible to conclude that in relation to V_{DS} equal to 0.8V, the I_{DS} / (W / L) of the OCTO MOSFET is 482% higher than that measured by the CM, thanks to the OCTO effects

The continuation of this work is implementing a new structure for the solar cell taking into account a base cell defined by the OCTO MOSFET that will be biased by using an external voltage source.

IV. Conclusion

In order to boost the electrical performance of the solar cells, an innovative structure is been proposed for its implementation which considers the use of OCTO MOSFETs biased. The next step of this work is to create this innovative structure of solar cell in the three-dimensional numerical simulation and perform the electrical characterization. Besides, we will perform a comparative study of this new structure with the typical one, regarding the same areas.

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