CMOS Power Amplifier with Adaptive Biasing and a 24.5 dBm OCP_{1dB}

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***Abstract*—This work presents a 2.45 GHz power amplifier (PA) using cascode topology in a 130 nm CMOS process. The same PA core is tested in two different cases. The first one corresponds to a dual-mode configuration where mode selection is achieved through the external application of bias voltages. In high power mode, this amplifier has an output power at 1 dB compression point (OCP_{1dB}) of 24.4 dBm and power added efficiency (PAE) at OCP_{1dB} of 16.3%. With the objective of improving both the linearity and the efficiency of the circuit, a second topology with an adaptive biasing cell was implemented for one of the amplifier cells. Its output voltage increases as the input power increases, varying between 1.17 V and 2.71 V. As a result, it was possible to obtain an amplifier with OCP_{1dB} of 24.5 dBm and PAE at OCP_{1dB} of 19.0%.**

***Index Terms*—adaptive biasing, power amplifier, linearity**

I. Introduction

One of the biggest concerns in telecommunications is the power consumption of its devices. Since many of these are powered by batteries, the circuits' efficiencies are directly connected with its usage time (when the battery is discharged) and with its life cycle (number of battery recharges). The most power consuming block of the radio frequency transceiver is the power amplifier (PA). In this context, the implementation of techniques that can improve both efficiency and linearity of the amplifiers is a necessity, as it will impact directly the device.

A multimode PA, as presented in [1-3], is a circuit architecture that enables the amplifier to have multiple modes. These modes can be selected by different bias voltages, obtaining different gains and output power values to each bias point. Adjusting the bias points accordingly to the current application, it is possible to improve the amplifier efficiency at power backoff.

However, these modes are usually selected by the circuit's device application with the help of external digital circuits, increasing the complexity of the final circuits with which the PA will be integrated. One way to solve this problem is using adaptive biasing cells, directly integrated with the PA. These cells have the function to change the amplifier bias point using the information provided by the input power - higher input power implies in higher biasing voltages, setting the amplifier to both low power and high power modes automatically, making external circuits no longer necessary. Examples of adaptive PAs can be seen in [4] and [5]. These works also show the flexibility of this technique, with one circuit using only NMOS transistors

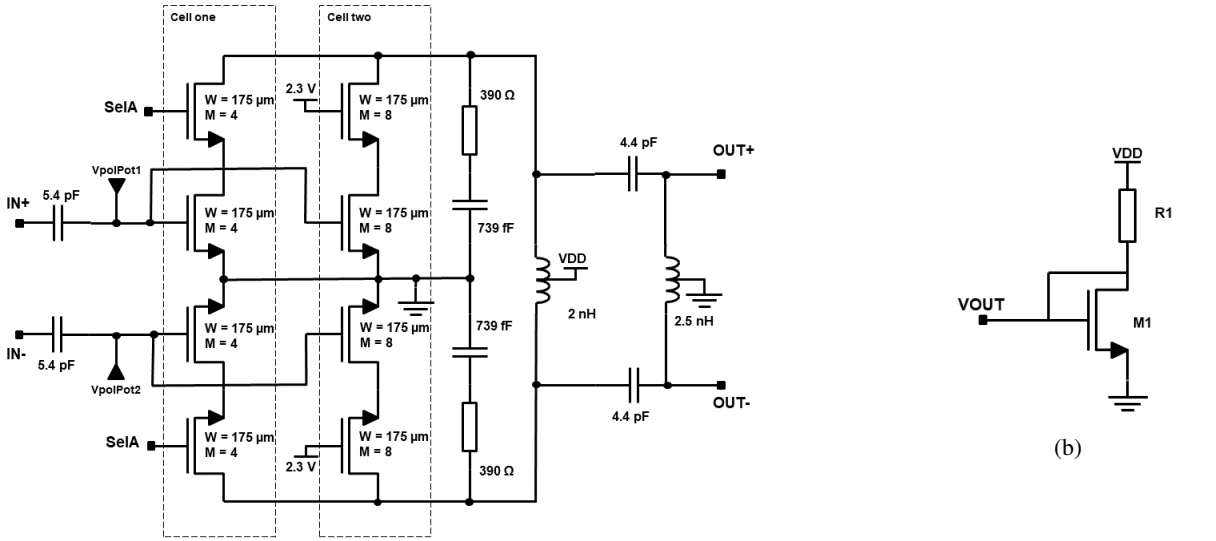
This paper presents the same PA core tested in two different cases. The first case is a dual-mode configuration, where different power modes are achieved through the external application of bias voltages, changing the output power values of the amplifier. After it, a new topology is proposed, substituting the external voltages with an internal circuit utilizing the structure described in [6], whose function is to adaptively bias the transistors of the amplifier. Both designs for the power amplifier and the adaptive bias cell are described in Section II. The simulation results of the power amplifier with and without the adaptive bias cell are shown in Section III.

II. Circuit Design

A. Power Amplifier

Fig. 1 (a) shows the schematic for the PA. The amplifier is composed of two parallel unit powers cells. These cells uses almost identical thick oxide transistors, only differing in multiplicity, resulting in a different effective channel width for each mode. The channel length is 240 nm. Each unit power cell is composed of a cascode differential pair. The circuit also has a feedback network made up of a resistor and a capacitor, to increase the stability, and an output matching network formed by a high pass LC configuration. All the capacitors on this circuit (as well as the capacitors on Fig. 2) are dual-dielectric metal-insulator-metal (MIM) capacitors. The circuit is powered by a 3.1 V voltage through V_{DD}.

The unit channel width for all the transistors is 175 μm. Turning the first cell on or off (applying a low or high voltage in SelA), the effective channel width of the amplifier changes, resulting in different values of gain and output referred power at 1 dB compression point (OCP_{1dB}). When SelA is connected to ground potential, the performance of the amplifier to low input power is satisfactory, but it quickly reaches its saturation point as the input rises. SelA is then connected to a higher voltage, which makes it work for a larger range of input power and raises the amplifier's gain and OCP_{1dB}, and ends up working for a bigger range of input power values.



(a)

Fig. 1: (a) Schematic of the power amplifier. (b) Internal circuit for bias voltage.

As presented in Fig. 1, cell's two transistor have a bigger multiplicity value than cell's one. As such, turning cell two on and off has a higher impact in the circuit results.

Another important point to notice in the presented circuit is the presence of central tap inductors. Considering the matching network and transistors biasing, four inductors are necessary ins this circuit. Since this work is a differential amplifier, all inductors are symmetric, therefore, it is possible to substitute each pair of inductors with central tap inductors with double of value of the former's inductante. With this change, the total number of inductors halved, and while the new inductors are bigger than the originals ones, the occupied area by all the elements in an layout was lowered.

Fig. 1 (b) shows the circuit used to provide the bias voltage labeled as VpolPot1 on Fig. 1 (a). In this architecture, the NMOS transistors are connected as diodes, creating an voltage divider. The advantage of using a transistor instead of a common resistor is the difference of space occupied by the two components, since in most cases the transistor will be able to achieve the same output voltage while occupying a smaller space.

B. Adaptive biasing

Fig. 2 presents the cell responsible for providing the adaptive voltage, with the structure proposed by [6]. The circuit starts to work from a threshold voltage, defined by both V_1 and components' values. When the input is below the threshold, M1 does not conduct current, and the output voltage SelA assumes the V_{BIAS0} value. When the input voltage increases past the threshold, M1 conducts, reducing the gate voltage of M2, which was initially set as V_{DD}. Due to the configuration of the transistor, reducing gate voltage of M2 implies in the output voltage raising, with its precise value varying with the component's values. In this circuit, M3 is used as a discharge path to reduce distortion caused due to the adaptive bias. The connection between body and drain on this transistor is used to make a p-n junction diode between body and source without any additional components, while also decreasing the discharged time of this circuit. The maximum output voltage of this cell can be controlled by changing the value of V_2. Note that V_2 is not the maximum output voltage of the circuit, as this supply alone can only control the maximum value to a certain point. To have a specific maximum value, another parameters of the circuit need to be changed.

Because of this behavior, it is possible to bias cell one from the amplifier (biased by SelA) adaptively. Initially, the power amplifier is biased with SelA fitted to low input powers. As the input rises, SelA rises as well, biasing cell one to a mode more fitted to high input powers. As such, the cell is used in both off and on states automatically, without any digital circuit

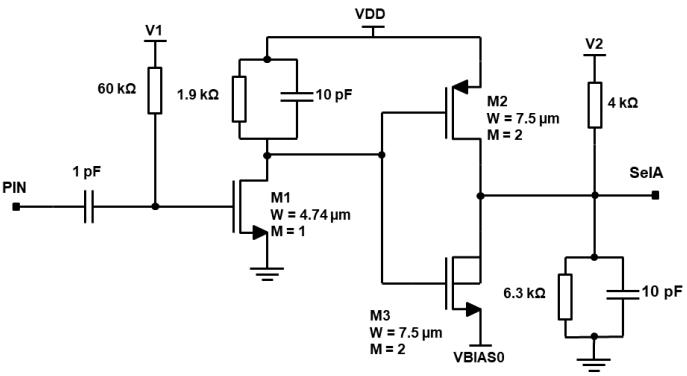


Fig. 2: Schematic of the adaptive biasing circuit.

TABLE I: Comparison between adaptive biasing and usual biasing

Cell one	OCP_{1dB} **(dBm)**	**Gain (dB)**	**PAE at** OCP_{1dB} **(%)**	**Maximum PAE (%)**	**Saturation power (dBm)**
Low power mode	21.6	7.8	11.3	12.0	21.8
High power mode	24.4	10.6	16.3	19.3	24.5
Adaptive bias	24.5	7.9	19.0	19.3	26.2

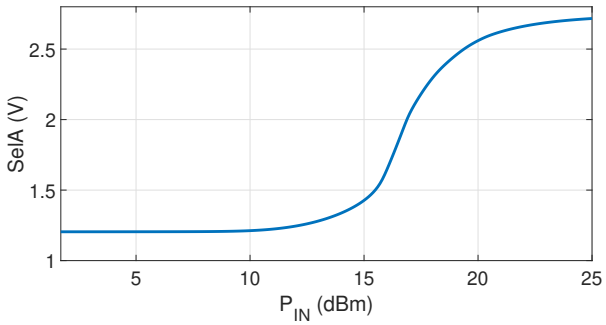


Fig. 3: Adaptive voltage versus input power.

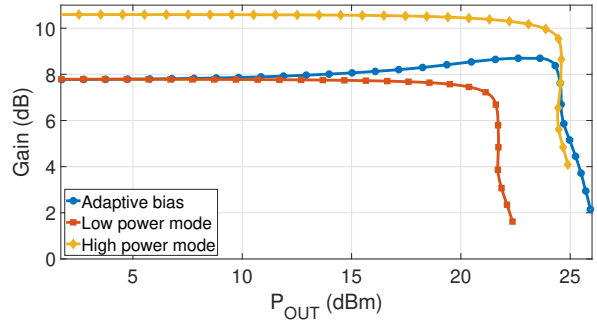


Fig. 4: Amplifier gain in three different states versus output power.

being connected to the amplifier.

This cell was designed by defining the input power threshold near to the input referred power at 1 dB compression point. In this case, the cell will achieve a higher voltage when the original gains starts compressing, compensating its decrease and, ideally, keeping the gain nearly constant until the input power reaches the compression point of the final circuit.

III. Simulation Results

All the results were validated using harmonic balance simulations, with the Cadence Spectre RF simulator. The biasing voltage of the amplifier's transistors (VpolPot) is 1.17 V. The output voltage for the adaptive biasing cell is SelA. The values for V_1, V_2 and V_{BIAS0} are, respectively, 0.49 V, 2.3 V and 1.17 V. All these voltages were provided by internal circuits, with the same architecture as Fig. 1 (b). For the simulations, the input power varied between -5 dBm and 25 dBm.

Three tests were made: two without the adaptive cell, applying both 0 V (low power mode) and 2.3 V (high power

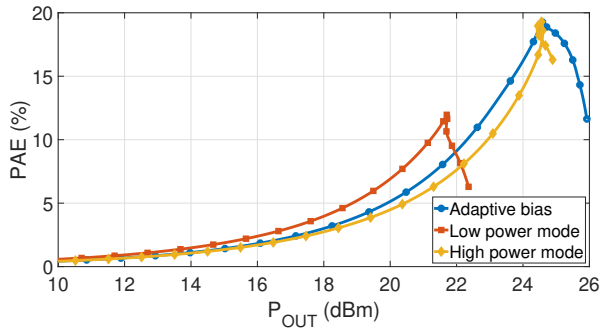


Fig. 5: Amplifier PAE in three different states versus output power.

TABLE II: Performance comparison of CMOS Linear Power Amplifiers

References	[7]	[8]	[9]*	This work*
Technology	180nm	180nm	350nm	130nm
Freq. (GHz)	2.40	2.40	2.40	2.45
Gain (dB)	24.6	14.0	29.4	7.9
OCP_{1dB} (dBm)	23.0	21.8	25.3	24.5
PAE at OCP_{1dB} (dBm)	27.0	30.4	—	19.0

* Validated through simulations.

mode) to SelA on the power amplifier, and one using only the adaptive bias circuit. The objective is to compare the results of the amplifier with and without the adaptive biasing.

Fig. 3 shows the SelA voltage versus the output power. For low powers, the output voltage is 1.17 V and reaches its high state with P_{IN} of 17.9 dBm, when the final output voltage is 2.71 V. Fig. 4 shows the amplifier gain in three different states of operation versus the output power. Fig. 5 shows the amplifier power added efficiency (PAE) in three different states of operation versus the output power. Table I details the values of gain, PAE and OCP_{1dB}.

As expected, for low input powers, using the adaptive biasing and SelA connected to ground potential results in almost the same gain. When input power rises, it is noticeable that the state where cell one is off starts to lose linearity. At this point, the adaptive biasing circuit is activated, providing a biasing voltage near to 2.3 V. With this, the amplifier keeps working properly for a higher range of output power values, improving the compression point in comparison to cell one off and on, as seen in Table 1.

The circuit with adaptive bias improves PAE at OCP_{1dB} in

comparison to the low/high power mode, with an improvement of 2.7 p.p. Actually, for every output power value, the PAE for the PA with adaptive bias is better than the high power mode, with the maximum difference of 2.25 p.p. for a 23.5 dBm output power. The saturation power also significantly improves, having an 1.8 dB improvement from the high power mode, showing that this design can successfully provide power for more demanding scenarios.

It is important to notice that the voltage for low input power provided by the adaptive biasing cell is 1.17 V, and not 0.00 V, as for the dual-mode PA. This change happens because the structure used cannot provide such a low output voltage. Because of that, the SelA voltage was chosen to make the circuit able to provide a similar gain when compared to the lower power mode. This different voltage, however, causes an imperfection on the PA's linearity, raising the gain from 7.8 dB to 8.7 dB. Even though this gain expansion appears, the results of the new circuit are superior to the original, justifying its adoption in this project.

Table II depicts the performance comparison between this work and others PAs that utilize adaptive bias circuits on its schematics.

The biggest difference from this work to the others papers presented is the gain, which is reasonable since the power amplifier presented here only have one stage, in comparison to the two-stage PAs from the other papers. This work also presented one of the best OCP_{1dB} from the comparisons.

IV. Conclusion

A 2.45 GHz power amplifier with an adaptive bias circuit in the 130 nm CMOS process was presented. The final circuit provided a gain of 7.9 dB, an OCP_{1dB} of 24.5 dBm and a PAE of 19.0% at OCP_{1dB}. With the adaptive biasing, the amplifier works properly with both low and high input power without the necessity of external digital circuits. The saturation power had an 1.8 dB improvement in comparison to the high power mode of the amplifier, showing another advantage of using the adaptive biasing cell. Therefore, the adaptive biasing cell worked well, being able to bias cell one without using external circuits and improving both efficiency and linearity of the amplifier.

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