Digital Control Circuit for Offset Calibration in CMOS Comparators

João Lucas Johan Brum and Paulo César C. de Aguirre
Universidade Federal do Pampa - UNIPAMPA
Centro de Tecnologia de Alegrete – CTA
Grupo de Arquitetura de Computadores e Microeletrônica - GAMA
Alegrete, Rio Grande do Sul, Brasil
Email: joaobrum.aluno@unipampa.edu.br, pauloaguirre@unipampa.edu.br

***Abstract*—This paper presents the simulation results of a calibration algorithm to compensate for the offset of CMOS comparators. This calibration scheme is based on the trimming of a 5-bit capacitor bank connected at each comparator output. The digital control block was coded in SystemVerilog and an AMS simulation validated the digital calibration logic using a double-tail dynamic comparator as a study case. The comparator was designed in a 180-nm CMOS process and the input offset voltage was emulated by an unbalanced output capacitance that generated an offset of 3 mV. The calibration scheme reduced the offset down to 500 μV.**

I. Introduction

Analog-to-digital converters (ADCs) are key building blocks in the signal acquisition chain for digital signal processing. Most ADC architectures have at least one comparator in their circuitry and current low-power ADCs are mainly based on dynamic comparators in complementary metal-oxide-semiconductor (CMOS) technology. The most used comparator topologies are: StrongArm, dynamic latched comparator, double-tail, Lewis-Grey, and differential pair comparator [1].

For high-speed ADCs like the flash ADC the comparators need to operate at high speed, and they play an important role in comparing the input signal with the reference voltages. The comparator has a limited settling time and could present an offset at its input due to imperfections in the manufacturing of components and asymmetries in the layout. When using CMOS technology this error is even greater [2]. To mitigate this problem, the use of circuits responsible for offset calibration in CMOS dynamic comparators is an approach adopted in many ADCs.

There are different calibration techniques to reduce the offset of CMOS comparators [3]. These techniques can be based on the control of the comparator output capacitance [4], on the bulk voltage control of the differential pair transistors [5], [6], or on the trimming of the differential pair itself [7]. All of these calibration techniques require a digital logic control circuit, usually designed with a hardware description language.

To study the aforementioned, this work presents the control algorithm for offset compensation of CMOS comparators. The adopted calibration strategy is based on the trimming of the comparator output capacitance. However, this method causes a limitation on the comparator speed due to the extra output capacitance. The algorithm was validated through AMS simulations and showed a significant reduction of the comparator input offset.

This work is organized as follows: Section II presents the calibration strategy, Section III presents the simulation results, and some conclusions are drawn in Section IV.

II. Calibration Strategy

A. Comparator topology

This calibration algorithm is designed to compensate for the offset of a low-voltage double-tail comparator [8]. This comparator topology was chosen because it is suitable for low-voltage applications since it has only three stacked transistors. The comparator was designed in a 180-nm CMOS process and will be used in a SAR ADC. The comparator schematic is shown in Fig. 1.

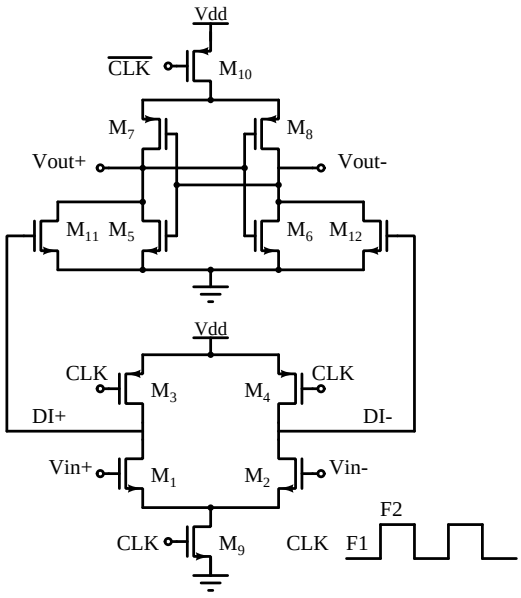


Fig. 1. Double-Tail Comparator.

The double-tail comparator has a pre-amplifier stage and a latch stage. Its working principle is explained as follows: the input stage is composed of transistors M_{1-4} and M_9. The input

signal is applied at the input pair transistors ($M_{1,2}$). During the reset phase (F1), transistors M_{3-4} are on and the nodes DI+ and DI− go to VDD, turning on transistors M_{11-12} and setting the output nodes at 0 V. During phase F2, the tail transistors (M_9 and M_{10}) turn on and the gate capacitance of transistors M_{11-12} drops according to the differential input signal, creating a small voltage difference between the nodes DI+ and DI−. This voltage difference is amplified by the cross-coupled inverters (M_{11-12}) and thus the output nodes are clamped to VDD and ground.

B. Calibration Approach

The calibration is performed by changing the output capacitance of the comparator output nodes [9]. During calibration the comparator inputs are disconnected from the input signals and are shorted together while connected to Vcm, as shown in Fig. 2. After the calibration, the comparator inputs are connected to the input signals.

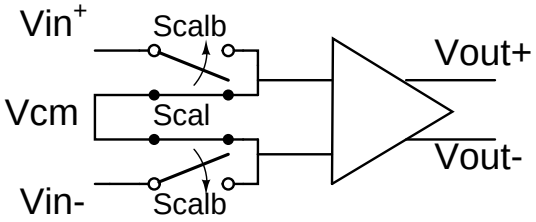


Fig. 2. Comparator and control switches.

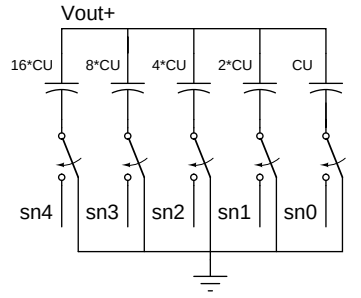
For calibration, a binary-weighted 5-bit capacitor bank is connected at each comparator output. These capacitor banks are represented in Fig. 3 and are controlled by the digital words sn and sp. The control logic circuit controls the number of capacitors that are connected at each output node. This calibration approach can compensate for positive and negative offsets. After the comparator inputs are shorted, the offset is estimated by measuring the comparator output state. To avoid switching due to noise, the comparator offset is estimated by an N number of comparisons (11 times in this work). After the offset sign (positive or negative) is estimated, the control circuit adds a capacitor in the respective output to reduce the offset magnitude. This procedure is repeated until the offset sign is changed. When the offset sign is changed the calibration algorithm stops.

The calibration time is dependent on the comparator input offset. It is a limitation of this calibration strategy.

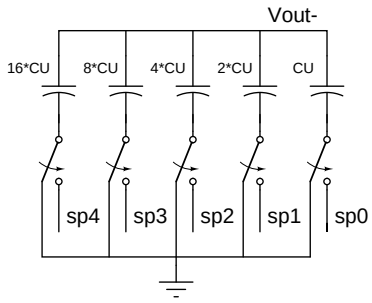
C. Logic Control Circuit

The calibration logic circuit was implemented with SystemVerilog and simulated with the ModelSim circuit simulator. After optimization, the final digital circuit algorithm is composed of a 7-state finite state machine (FSM), which is represented in Fig. 4.

In the first state, the FSM waits until all conditions are know, the $Reset$, $Clock$ and $Calon$ inputs must correspond to a high logic level. Then, the comparator inputs are shorted



(a) Positive Output



(b) Negative Output.

Fig. 3. Capacitor banks at the comparator outputs.

to start the calibration. The positive comparator output is applied at the control logic input and is represented as the Scompp variable. Then, 11 comparisons are performed to verify the offset magnitude. For this, auxiliary variables va and vb are used in states S1-S4. The collected data is used in a logical relation where the result is the capacitance value to be corrected. If the offset is positive, the variable sn is increased while sp is kept at zero logic. If the offset is negative, the sp variable is increased while sn is kept at zero.

Noteworth, if the comparator offset changes the polarity, the calibration ends. If no offset polarity changes are verified, the calibration stops when all 5 bits of the capacitor bank are at high logic level. When the calibration stops, the bit $Calok$ is set at high logic level indicating that the comparator is ready for operation.

III. Simulation Results

The calibration algorithm was tested to calibrate the offset of a low-voltage double-tail comparator running at 100 MHz. To save time and avoid a time-consuming Monte Carlo simulation to test the digital circuitry functionality, the comparator offset was emulated. Two different capacitors were connected at the comparator output to emulate an offset of -3 mV. This offset was emulated by using one capacitor of 10 fF and the other with 50 fF, thus creating a 40 fF mismatch at the output capacitance.

The offset was measured with the ramp method [10]. For this, one comparator input was set at Vcm (VDD/2) while the other input signal is a slowly variant ramp, from Vcm - 100 mV up to Vcm + 100 mV. Ideal capacitors and switches are used in this work. The unitary capacitor is 4 fF.

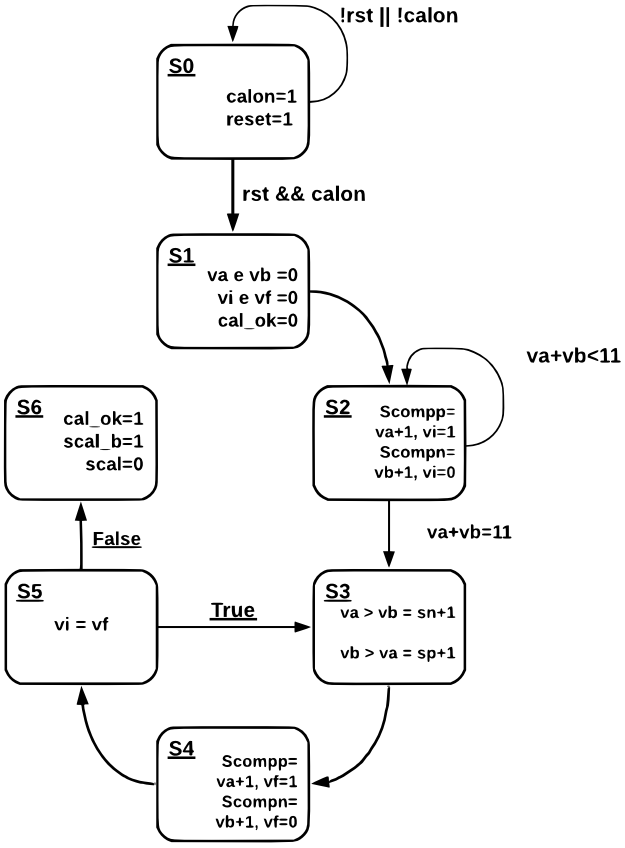


Fig. 4. State Machine.

An AMS simulation was performed to verify the functionality of the calibration circuit. After the comparator inputs to be set in Vcm, the calibration circuit started the search for the correct sp<4:0> and sn<4:0> signals. The final calibration signals are sn<4:0>= 00000 and sp<4:0> = 01011. It means that the extra capacitance added at the comparator output is $11 \times \mathrm{CU} = 44\mathrm{fF}$, leading to a total capacitance mismatch of 4 fF. After the calibration, the total comparator offset is 500 μV, as shown in Fig. 5.

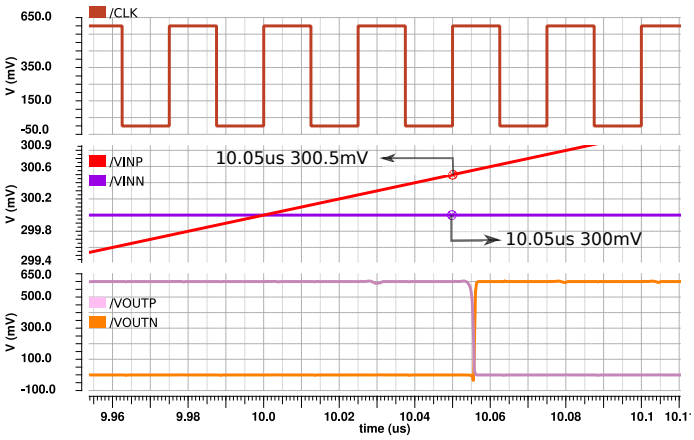


Fig. 5. Comparator offset after calibration.

The magnitude of the final offset is related to the unitary capacitor. Thus, for a lower offset a smaller unitary capacitor should be used.

IV. Conclusions

This work presented a calibration scheme for the offset compensation of CMOS comparators. The calibration algorithm changes the comparator output capacitance to compensate for mismatch and layout effects. The digital calibration algorithm was coded in SystemVerilog and its functionality was verified by an AMS simulation. It was possible to reduce the offset of a double-tail CMOS comparator from 3.5 mV to 0.5 mV. This precision is limited by the capacitor bank unitary capacitors. The drawback of this calibration strategy is the minimum number of clock cycles required to finish the calibration.

Acknowledgment

The authors would like to thank the Research Support Foundation of the State of Rio Grande do Sul (FAPERGS) grant PROBITI-FAPERGS-2020-2021.

References

[1] R. Sangeetha, A. Vidhyashri, M. Reena, R. B. Sudharshan, S. govindan, and J. Ajayan, "An overview of dynamic cmos comparators," in *2019 5th International Conference on Advanced Computing Communication Systems (ICACCS)*, 2019, pp. 1001–1004.

[2] Y. Feng, Q. Fan, H. Deng, J. Chen, R. Zhang, P. Bikkina, and J. Chen, "An automatic comparator offset calibration for high-speed flash adcs in fdsoi cmos technology," in *2020 IEEE 11th Latin American Symposium on Circuits Systems (LASCAS)*, 2020, pp. 1–4.

[3] F. Maloberti, *Data Converters*. Springer US, 2007.

[4] G. Van der Plas, S. Decoutere, and S. Donnay, "A 0.16pJ/Conversion-Step 2.5mW 1.25GS/s 4b ADC in a 90nm Digital CMOS Process," in *2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers*, 2006, pp. 2310–.

[5] E. Alpman, H. Lakdawala, L. R. Carley, and K. Soumyanath, "A 1.1V 50mW 2.5GS/s 7b Time-Interleaved C-2C SAR ADC in 45nm LP digital CMOS," in *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, 2009, pp. 76–77,77a.

[6] M. Yoshioka, K. Ishikawa, T. Takayama, and S. Tsukamoto, "A 10-b 50-MS/s 820- μW SAR ADC With On-Chip Digital Calibration," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 6, pp. 410–416, 2010.

[7] A. Varzaghani, A. Kasapi, D. N. Loizos, S.-H. Paik, S. Verma, S. Zogopoulos, and S. Sidiropoulos, "A 10.3-gs/s, 6-bit flash adc for 10g ethernet applications," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3038–3048, 2013.

[8] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, 2007, pp. 314–605.

[9] D. Li, Q. Meng, F. Li, and L. Wang, "An analysis of offset calibration based additional load capacitor imbalance for two-stage dynamic comparator," in *2016 6th International Conference on Information Communication and Management (ICICM)*, 2016, pp. 264–267.

[10] J. de la Rosa, *Sigma-Delta Converters: Practical Design Guide*. IEEE Press Wiley, 2018.