Digital Control of a Synchronous 8-bit SAR ADC

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***Abstract*—This work presents the implementation of a SAR logic control circuit for a synchronous 8-bit charge redistribution SAR ADC. The SAR logic algorithm is implemented using a finite stage machine and coded in SystemVerilog. The logic circuit validation was initially performed using the ModelSim simulator, and then with an AMS simulation in the Virtuoso Suite. An 8-bit SAR ADC running at 20 MHz with ideal capacitors and switches was used to validate the digital logic control circuit.**

I. Introduction

Analog-to-digital converters (ADCs) are used in several mixed-signal systems and system-on-chip (SoCs) designs. These converters work as a bridge between the analog world and the digital world, thus playing an important role in modern signal processing systems, together with the digital-to-analog converters (DACs) [1].

There are many ADC architectures as such as Flash, Sigma-Delta, Dual-Slope, Pipeline and the Successive Approximation Register (SAR) ADC [2]. Among those architectures, the SAR ADC has a wide use for low-speed and low-power consumption applications. The architecture can be used in industrial process control, optical communication and biomedical systems. In these applications, it is often necessary to digitize the data generated by a large number of sensors. The SAR ADC is also a good candidate for Internet of Things (IoT) and ultra-low-voltage (ULV) applications [3].

The SAR ADC is composed of a sampling and hold circuit (S&H), a feedback DAC, a clocked comparator and a digital logic control circuit that implements the SAR logic [4]. Based on the results obtained in the comparison between the sampled signal and the DAC feedback, the digital control circuit determines the value of each ADC output bit successively, and sequentially, from the most significant bit (MSB) to the less significant bit (LSB) [5].

The charge redistribution SAR ADC was proposed in [6], [7], and today is widely used. Also, the SAR ADC operation can be synchronous or asynchronous [8]. Both implementations require a logic control circuit.

Thus, this work presents the control algorithm of an 8-bit synchronous SAR ADC implemented in SystemVerilog. This circuit is part of a 8-bit low-voltage and low-power SAR ADC under development.

This work is organized as follows: Section II presents the SAR ADC, Section III presents the logic control circuit, Section III presents the simulation results and some conclusions are drawn in Section V.

II. 8-bit SAR ADC Topology

The successive approximation conversion method allows for higher resolution than the parallel conversion methodology [9]. This type of conversion uses a feedback technique for relating an analog input voltage with a N-bit binary value. The SAR ADC requires $N + 2$ clock cycles to perform the conversion process. The simplified diagram of the 8-bit SAR ADC used in this work is shown in Fig.1. It is a single-ended implementation used to verify the designed control logic circuit.

The successive approximation algorithm starts by sampling the input signal and resetting the comparator output. Then, the MSB is set to a high logic value. Then successive approximation starts by connecting the capacitor $2^{\mathrm{N}-1}\mathrm{C}$ to *Vref*. Thus, the voltage at *Vtop* is compared with the common-mode voltage. Depending on the result of this comparison, the MSB will be kept at high logical level or will go to a low logic level. Then, the next capacitor $2^{\mathrm{N}-2}\mathrm{C}$ is connected to *Vref* and the whole process is repeated for until all 8 output bits are defined.

The logic control commands the beginning and the end of each approximation step. The ADC output is valid only when the output "EOC" is set to a high logic level, indicating when the entire conversion process is completed.

III. Logic Control Circuit

The SAR ADC logic circuit presented in [10] is well-known and widely used to date [11]. However, it is custom designed in most cases. To speed-up the design time and migration to different technology nodes, a SAR logic control circuit implemented in a hardware description language (HDL) is designed in this work.

The logic control circuit designed in this work has 3 inputs and 4 outputs (some of them are an 8-bit bus). The input pins are: clock input (clk), comparator output (comp) e reset (go). The outputs are: SH for sampling the input signal, value is the capacitors control signals (represented as s<7:0> in Fig. 1), result is the final result, and conv-ok indicates the end of the conversion.

This digital control circuit is designed with a 9-state finite state machine (FSM), shown in Fig. 2.

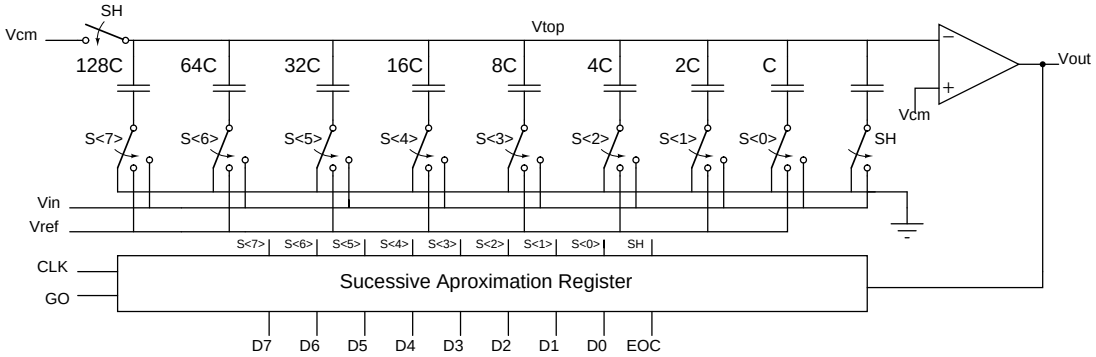

Fig. 1. Simplified schematic diagram of a 8-bit SAR ADC.

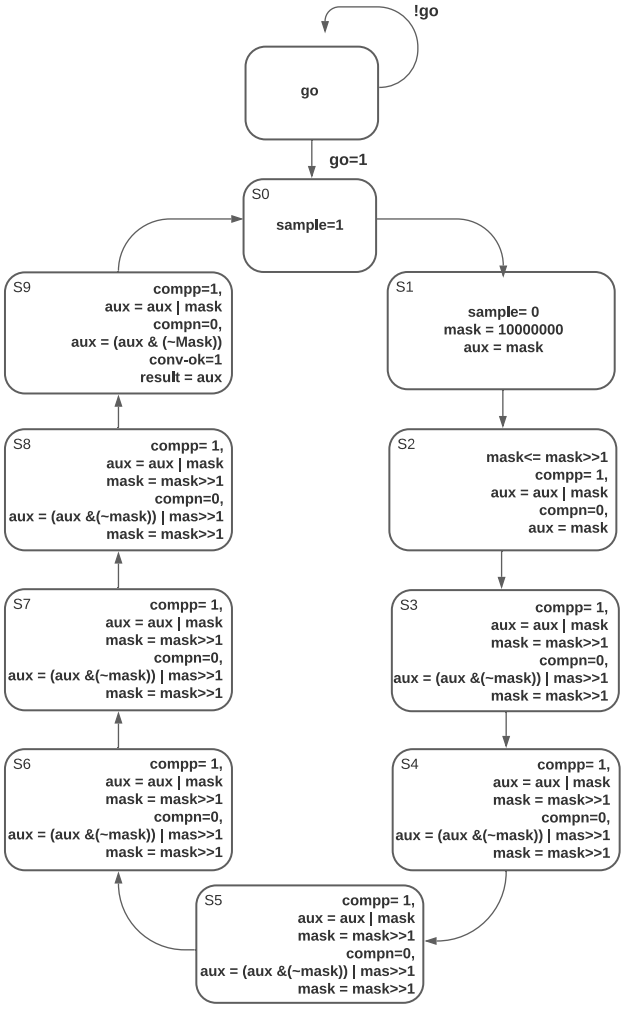

Fig. 2. Finite State Machine.

There is a reset phase while the signal *go* is at low logic value. If the signal *go* is at high logic level, the SAR logic starts. In the initial state, S0, the SH signal goes to "1" at the rising edge of the clock signal. At S1 state, the SH signal goes to "0" and the mask signal (Mask) receives "10000000". This current Mask value is stored in the auxiliary variable (Aux) to be directed to the DAC capacitors.

In the state S2, the mask value is updated with a shift to the right and the comparison takes place to determine the MSB value, this comparison takes place as follows: when the comparator output is at high logic level, the auxiliary variable receives an "or" (or logical) between previous Aux and Mask, otherwise, if the comparator output is at low logic level, the Aux variable will the receive Mask value. In state S3 when the comparator output is equal to "1", the Mask value is updated with the shift right and the auxiliary variable receives an "or" (or logic) between previous *Aux* and *Mask*, and when it is equal to zero the auxiliary variable will receive an "and" (logical and) of previous *Aux* and previous *Mask* negated and an "or" of this result with *Mask* shifted to the right. After the execution of this last algorithm the *Mask* value is shifted to the right.

The logic of state S3 is reproduced in states S4, S5, S6, S7 and S8. In state S9 only the LSB comparison is made, and if the comparator output is one, the auxiliary variable will receive Aux "or" Mask, and if it is zero it will receive Aux "and" Mask negated. In this state, the Result output receives Aux and the Conv-ok output is placed at a high logic level, thus giving permission to return to the initial state S0 to start the next conversion.

IV. Simulation Results

The SAR logic control circuit is validated by an AMS simulation on the Virtuoso Suite from Cadence. This type of simulation allows the simulation of analog circuits and digital blocks coded in hardware description language. However, this simulation is more time consuming and requires extra simulator setups. In this project, the goal is to design a low-voltage 8-bit SAR ADC. In this simulation, an ideal SAR ADC is considered. The capacitors and switches are ideal ones. The comparator is a verilogA implementation with no input offset. At this simulation, an ideal reference voltage of 1 V is considered. Thus, the ADC step size is equal to 0.00390625 V. The clock signal is set to 20 MHz.

The first transient simulation is for a constant input signal of 123.45 mV (aleatory value). Figure 3 shows the control signals in this transient simulation. The final result is 00011111, leading to an output signal equal to 121.0938 mV.

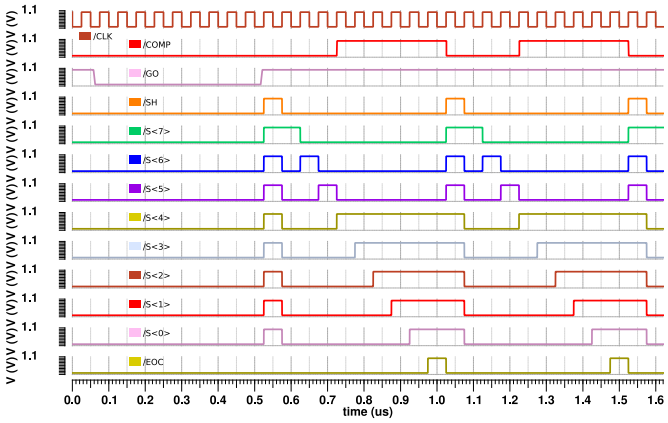

Fig. 3. Control logic signals for a constant input signal of 123.45 mV.

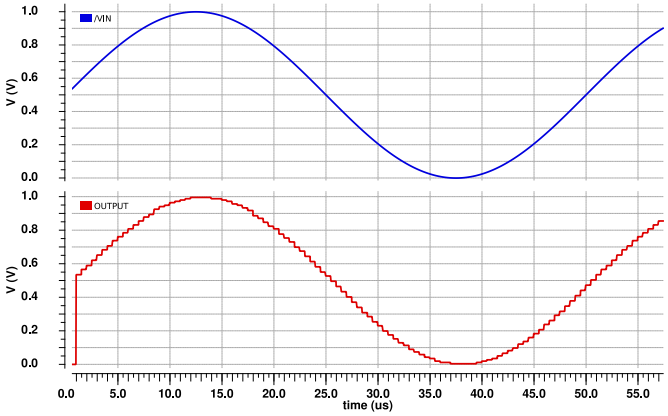

Fig. 4. ADC output signal.

The binary to decimal conversion is made by using a verilogA auxiliary block.

The second transient simulation considers a 20-kHz full-scale input signal. Figure 4 shows the ADC output for this transient simulation. Based on the results, we can conclude that the SAR ADC control logic is working and is ready for the optimum logic synthesis and layout process. Also, this algorithm can be easily changed for a higher resolution implementation. Preliminary logic synthesis results performed using the Cadence Genus Synthesis Solution indicate that the proposed circuit requires a total of 173 logic gates of a traditional standard cell library working at 1.8 V.

V. Conclusions and Future Work

This work presented the logic control circuit for an 8-bit SAR ADC. The control circuit was coded in SystemVerilog, verified with the ModelSim circuit simulator and then used in an AMS simulation of an ideal SAR ADC. This control logic can be expanded for a higher resolution ADC. The next steps is to perform the logic synthesis and layout of this control circuit so it can be used in a low-voltage 8-bit SAR ADC. Also, the fully-differential implementation of the SAR ADC will be performed.

Acknowledgment

The authors would like to thank the Research Support Foundation of the State of Rio Grande do Sul (FAPERGS) grant PROBITI-FAPERGS-2020-2021 and the UNIPAMPA Academic Development Program (PDA) 2021 grant.

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