A Low-Power 0.4-V Negative Resistance-Based Small-Signal Amplifier

Suzian Mahéli Ramos Santos, Madaglena Mbuy Miko Mikue, Lucas Compassi-Severo
Computer Architecture and Microelectronics Group - GAMA
Federal University of Pampa, Alegrete Campus
Alegrete, Brazil
{suziansantos.aluno, madaglenamikue.aluno, lucassevero}@unipampa.edu.br

***Abstract*—The Internet of Things (IoT) evolution has required the design of power-optimized circuits in order to improve the lifetime of the battery-powered circuits. Based on that, several novel topologies of analog and digital circuits have been proposed in the literature with a focus on low-power operation. In this paper, the implementation of low power and low voltage amplifier is proposed using the effect of negative resistance. The proposed circuit is analyzed and designed in the TSMC 180 nm CMOS technology to work with only 0.4 V of power supply. Simulation results have shown the ability to provide up to 250 V/V of voltage gain and to present a unity gain frequency of up to 20 MHz when the power dissipation is around 500 nW. The variable gain capability was also analyzed by changing the resistance values. The results show that it is possible to provide voltage gain from 22 to 42 dB and a unity gain frequency of 1 MHz, with a capacitive load of 1 pF.**

***Index Terms*—low power amplifier, low voltage operation, negative resistance.**

I. Introduction

The Internet of Things (IoT) presents the potential for dramatic improvement in the most diverse areas in which it is applied, from monitoring machines on the factory floor to treating chronic diseases such as diabetes. Also, a great economic impact of up to 11.1 trillion per year by 2025 is estimated for IoT applications, according to [1]. This means an impact on the world economy of about 11%. To achieve this level of development the organizations that manage this technology will have to overcome technical obstacles to better tools and methods [2].

Circuit power consumption is one of the main challenges of IoT devices. It limits the circuit lifetime and the application of IoT in some energy-constrained scenarios, like wireless sensor networks and implantable devices. Thus, the power optimization and the design of novel circuit topologies are very important to design IoT circuits [2].

Voltage amplifiers are analog basic building blocks that can be employed in several IoT low-power applications, such as RF receivers, active filtering, and instrumentation. In general, they are implemented in the CMOS process using classical topologies such as common-source amplifiers, multi-stage operational amplifiers, and fully-differential amplifiers. However, these topologies present considerable power dissipation even at low-frequency operation [3].

Some novel amplifier topologies have been proposed in the literature by using active negative conductance circuits to compensate for the low voltage gain and reduced bandwidth of the amplifier without increasing the power consumption [4], [5]. In [3] and [5] a low voltage negative transconductance circuit is employed at the inputs of the single-stage fully differential amplifier to implement complex filters and variable gain amplifier to be used in low-energy RF receivers.

The use of the negative conductance effect is now new, since the sixties, discrete tunnel diodes have been used to implement high-frequency amplifiers [6], [7]. The implementation of these circuits in the CMOS process can be performed with active circuits single-ended or differential circuits to emulate the negative conductance [8].

In this paper, we intend to analyze the use of negative resistance to provide signal amplification from a simple voltage divider circuit. Its operation is very similar to the classical tunnel diode amplifiers used in high-frequency applications, but we propose the use of a CMOS cross-coupled negative transconductor to produce the negative resistance. The circuit is implemented in the CMOS 180 nm process to operate with power dissipation on the nW scale with a power supply of 0.4V.

This paper is organized as follows: after the introduction, the presentation and definition of a Negative Resistance-based amplifier are presented in Section II. In Section III the cross-coupled negative tranconductor is analyzed and Section III presents the simulation results. Finally, Section IV presents some conclusions based on the obtained results and proposed some future works.

II. Negative Resistance-Based Amplifier Analysis

The negative resistance-based amplifier proposed in this work can be analyzed by means of the simple voltage divider circuit presented in Fig. 1. It is composed of two resistors (R_1 and R_n). The transfer function of this circuit can be evaluated by equation 1.

$$A_V = \frac{Vout}{Vin} = \frac{R_n}{R_1 + R_n} \tag{1}$$

If only positive resistors are used, the transfer function is always working as a voltage attenuator, since the denominator

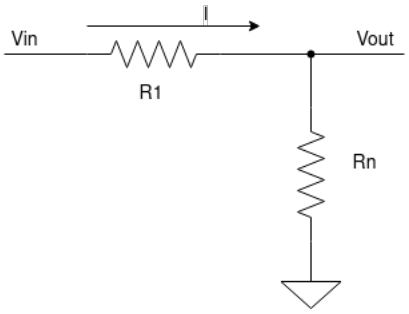

Fig. 1. Basic circuit for negative resistance gain analysis.

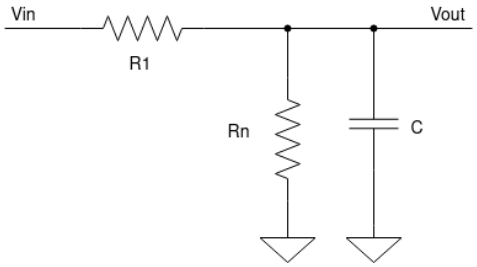

Fig. 2. Circuit for gain analysis with negative resistance in parallel with capacitor.

is always higher than the numerator. On the other hand, if R_n presents the behavior of negative resistance, the equation denominator can reach values lower than the numerator and the circuit can work as a voltage amplifier. The voltage gain level can go to infinity when R_n tends to -R_1. Additionally, it is important to note that if R_n is lower than -R_1 the amplifier works with positive gain but if R_n is higher than -R_1 the voltage gain is negative.

The input impedance is also affected by the negative resistance and goes to zero when R_n tends to -R_1, as shown in equation 2. Thus, in practical applications, a finite gain should be employed to keep the input impedance higher.

$$Z_{in} = R_1 + R_n \tag{2}$$

In general, this circuit will drive some capacitance load and the negative resistance implementation will present some parasitic capacitances at its nodes. Thus, as shown in figure 2, the effect of a capacitance connected in parallel to R_n should be evaluated. Equation 3 shows the voltage gain as a function of the Laplace frequency. As expected it presented a single-pole behavior in which the pole frequency is given by equation 4. The pole frequency is proportional to $R_1 + R_n$, presenting lower values when the amplifier has a higher gain level. The input impedance is also affected by the capacitor, as shown in 5.

$$A_V(s) = \frac{R_n}{s.R_1.R_n.C + R_1 + R_n} \tag{3}$$

$$\omega_p = \frac{R_1 + R_n}{R_n.R_1.C} \tag{4}$$

$$Z_{in} = R_1 + \frac{R_n}{s.R_n.C + 1} \tag{5}$$

The negative resistance-based amplifier can have its gain changed by the resistor R_1 or by the negative resistance value R_n. As shown by Eq. 2 the input impedance is proportional to the difference between R_1 and R_n. Thus, higher values of input impedance are obtained only for lower values of voltage gain.

III. Cross-Coupled Negative Transconductor

In this project, the implementation of the negative resistance is based on the cross-coupled negative transconductor topology. Its schematic is shown in figure 3. This topology is composed of two PMOS transistors, with equal W/L ratio, functioning as cross-coupled transconductors and two NMOS transistors work as current source loads [3]. The transistor M5 work as an active diode in order to mirror the I_{ref} current to the M3 and M4 transistors.

The small-signal model of this circuit gives us symmetrical input voltages because it is a differential circuit. Equations 6 and 7 shows the equivalent output current in both terminals in^+ e in^-. In these equations g_{m1} and g_{m2} represent the transconductances of M_1 and M_2, g_{ds1} and g_{ds2} the output conductance of M_1 and M_2 and g_{ds3} and g_{ds4} the output conductance of M_3 and M_4.

$$g_{m1}.v_{in^-} + g_{ds4}.v_{in^+} + g_{ds1}.v_{in^+} = i_{in^+} \tag{6}$$

$$g_{m2}.v_{in^+} + g_{ds3}.v_{in^-} + g_{ds2}.v_{in^-} = i_{in^-} \tag{7}$$

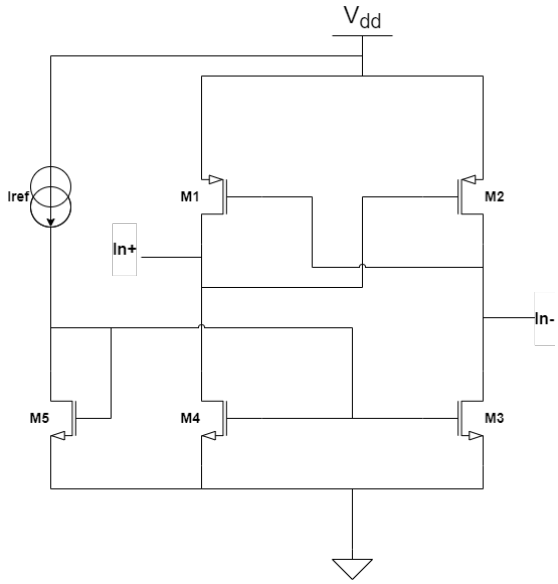

Fig. 3. Negative transconductor with Cross-Clouped and current mirror.

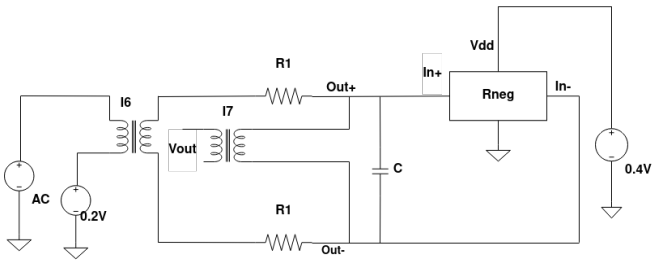

Fig. 4. Circuit Test-bench used for simulation.

Subtracting (7) from (6) and considering the $g_{m1} = g_{m2} = g_m$, $g_{ds1} = g_{ds2} = g_{dsP}$, $g_{ds3} = g_{ds4} = g_{dsN}$ and $v_{in^+} = -v_{in^-}$, the small signal equivalent negative resistance (R_{neg}) at the circuit can be obtained as shonw in 8.

$$R_{neg} = \frac{v_{in^+} - v_{in^-}}{i_{in^+} - i_{in^-}} = -\frac{1}{g_m + g_{dsP} + g_{dsN}} \tag{8}$$

The value of R_{neg} can be adjusted according to the DC voltage level, the transistor sizes, and the I_{ref} current level. The DC voltage of the input terminals should be at the level of $V_{DD}/2$ to improve the dynamic range. As shown in the previous section, the design should be performed to obtain the $|R_{neg}|$ near R_1 in order to obtain a high voltage gain.

IV. Simulated Results

As shown in sections II and III the objective of this work is to analyze and design the voltage amplifier based on the negative resistance. The negative resistance is implemented with the cross-coupled transcondutor. Due to this, a fully differential amplifier should be designed, using two voltage divider blocks.

For this design, the TSMC CMOS 180nm process is used and the circuit is designed to operate with the supply voltage of 0.4 V. The resistor of the amplifier (R_1) was chosen to be 100 kΩ, due to that the R_{neg} should be designed to be near -100 kΩ, resulting in a negative conductance of 10 μS. In order to avoid circuit instabilities and to present a positive voltage gain the design of the transconductor was performed to obtain R_{neg} ≈-102 kΩ. At this level, the low-frequency input impedance of the circuit is around $1k\Omega$, as defined by Eq. 2.

The transistors of the circuit from Figure 3 were sized following the method proposed in [9], where the transistor characteristics curves were adopted to obtain the current density and the transistor aspect ratio (W/L). The $|V_{GS}|$ and $|V_{DS}|$ are tied to 0.2 V in order to operate with a V_{DD} of 0.4 V. Table I shows all the design parameters used for the results shown in this paper.

The simulations were performed on the Cadence Virtuoso Environmental using the test-bench shown in the schematic of Figure 4. At the input and output, two ideal baluns were used to perform the single-ended to differential and differential to single-ended conversion. The input DC voltage level was defined as 0.2 V in order to bias the circuit input and a source of 0.4 V was used to supply the circuit. The power consumption of the proposed amplifier, measured at the operation biasing point for maximum gain, is equal to 557.4 nW.

TABLE I
Parameter values for the designed circuit.

Parameters	Value	Unit
W_N	4.8	μm
L_N	1.0	μm
W_P	16.5	μm
L_P	1.0	μm
I_{ref}	464.5	nA
R_1	100	$k\Omega$
R_{neg}	≈ -102	$k\Omega$
g_{mP}	10.18	μS
g_{dsP}	237.3	nS
g_{dsN}	115.5	nS

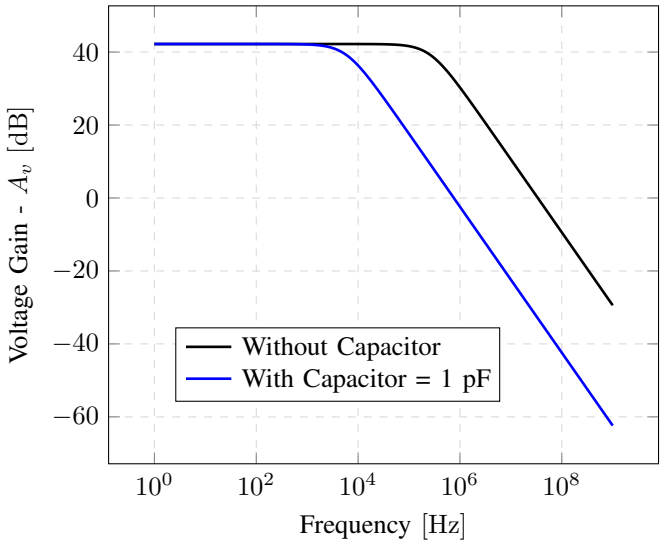

Fig. 5. Voltage gain as a function of the frequency, without capacitance and with a capacitive load of 1 pF.

Figure 5 shows the voltage gain as a function of the frequency of the designed amplifier. As could be seen the low-frequency gain obtained is about 41 dB. The unity gain frequency is near 20 Mhz without any capacitive load and it is reduced to about 900 kHz when a differential capacitive load of 1pF is added between the outputs.

To analyze the effect of the $R_1 - R_n$ difference on the voltage gain, parametric simulations were executed to change the R_1 value from $90k\Omega$ to $100k\Omega$. The result of this simulation is shown in Figure 6. The curve shows the variation of the voltage gain from 0 to 250 V/V due to the difference $R_1 - R_n$. At $R_1 = -R_n$ the voltage gain can go to infinity, but it is not shown in this figure due to the variation step adopted. It can be verified that the voltage gain changes approximately symmetric for $R_1 < -R_n$ and $R_1 > -R_n$, however at the $R_1 = -R_n$ occurs a phase inversion.

Figure 7 shows the frequency response for values of R_1 from 95 $k\Omega$ to 101.5 $k\Omega$. As can be seen, the gain is changed from 22 dB to 42 dB. For this simulation, the differential

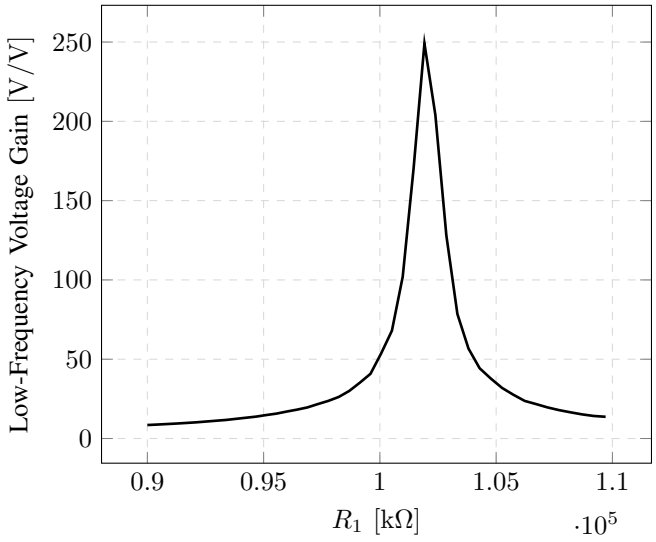

Fig. 6. The variation of the voltage gain according to the R_1 value.

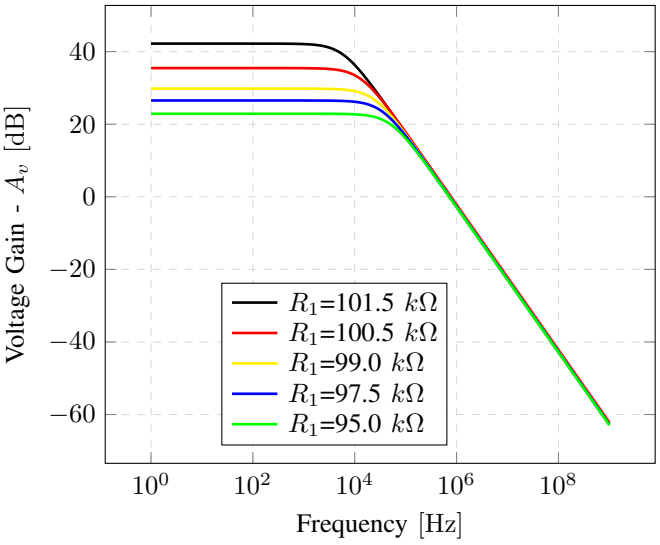

Fig. 7. Frequency response of the amplifier for different values of R_1.

capacitive load of 1 pF is used and the unity frequency is kept constant is approximately 900 MHz. It is interesting to show that the proposed amplifier can work as a variable gain amplifier by changing the R_1 resistor value.

Table II shows a comparison of the results of this work with other low-power amplifiers from the literature. The amplifier proposed in this work presented the lowest power dissipation and a higher voltage gain among the compared works. Besides the lower power dissipation, the bandwidth obtained is comparable to those obtained in other works.

TABLE II
COMPARISON WITH OTHER LOW-POWER AMPLIFIERS

References	This Work	[12]	[11]	[10]
Power (μW)	0.55	8.9 $\rightarrow$ 15.4	56	55
Gain (dB)	0 $\rightarrow$ 42	0.2 $\rightarrow$ 18.4	-14/33	4/55
Bandwidth (MHz)	0.05 $\rightarrow$ 0.9	0.98 $\rightarrow$ 2.85	5.0	0.54
Supply Voltage (V)	0.4	0.36	1.0	1.0
Technology (nm)	180	180	90	130

V. CONCLUSION

In this work, a negative resistance-based amplifier was proposed for low power and low voltage circuits. The proposed amplifier is composed of only a pair of resistors and a cross-coupled negative transconductor circuit. The circuit was designed in the TSMC 180nm CMOS process to work with a voltage supply of 0.4 V. The simulation results have shown a power dissipation of only 557.4 nW and the amplifier can provide up to 250 V/V of voltage gain. The unity frequency was 20 Mhz without capacitive load and about 1 MHz with a capacitive load of 1pF.

This preliminary analysis of the proposed amplifier shows the promising capability of a novel implementation of low-power amplifiers, presenting improved results in comparison to other works from the literature.

In future works, we intend to design the circuit layout, evaluate the circuit under process, voltage and temperature variations (PVT), evaluate strategies to improve the input impedance at higher voltage gains and make a prototype of the circuit for experimental validation.

REFERENCES

[1] MANYIKA, James. The Internet of things, avaiable on: https://www.mckinsey.com/mgi/overview/in-the-news/by-2025-internet-of-things-applications-could-have-11-trillion-impact, 2015.

[2] E. Kargaran, D. Manstretta and R. Castello, "Design Considerations for a Sub-mW Receiver Front-End for Internet-of-Things," in IEEE Open Journal of the Solid-State Circuits Society, vol. 1, pp. 37-52, 2021.

[3] SEVERO, L. Compassi, Van Noije, W, A 0.4-V 10.9- W/Pole Third-Order Complex BPF for Low Energy RF Receivers, IEEE Transactions on Circuits and Systems I: Regular Papers, 66 (6), 2, 2019.

[4] Ananda Mohan, P. (2020), Analysis of negative-R assisted integrators and differentiators. Electron. Lett., 56: 123-125, 2020.

[5] SEVERO, L. Compassi, Van Noije, 0.36 V PGA combining single-stage OTA and input negative transconductor for low energy RF receivers, Electronics Letters, 54 (5), 319-320, 2018.

[6] AMATO, Francesco et al. Long range and low powered RFID tags with tunnel diode. In: 2015 IEEE International Conference on RFID Technology and Applications (RFID-TA). IEEE, 2015. p. 182-187.

[7] TANG, Qi; XIN, Hao. Stability of tunnel diode based negative impedance circuit. In: 2014 USNC-URSI Radio Science Meeting (Joint with AP-S Symposium). IEEE, 2014. p. 131-131.

[8] SHEIKHOLESLAMI, Ali. Negative resistance [circuit intuitions]. IEEE Solid-State Circuits Magazine, v. 6, n. 4, p. 7-8, 2014.

[9] GIRARDI, A. G., Compassi-Severo, L, de Aguirre, P. C. C., Design Techniques for Ultra-Low Voltage Analog Circuits Using CMOS Characteristic Curves: a practical tutorial, Journal of Integrated Circuits and Systems, vol. 17, n.1, 2022.

[10] Masuch, J. and Delgado-Restituto, M., A 1.1-mW-RX 81.4-dBm Sensitivity CMOS Transceiver for Bluetooth Low Energy, IEEE Trans. on Microwave Theory and Techniques, 61, (4), pp. 1660-1673, 2013.

[11] Zhou, C., et al., A 56uW VGA with 5MHz bandwidth and 47dB gain-range in 90nm CMOS, Proc. of International Symposium on VLSI Design, Automation and Test (DATE), March 2010, pp. 91-94.

[12] Severo, L. and Van Noije, W., 0.36 V PGA combining single-stage OTA and input negative transconductor for low energy RF receivers, Electron. Lett., 54: 319-320, 2018.