Loadpull simulations of a CMOS stacked power amplifier with 16QAM IEEE 802.11ax signals

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***Abstract*—This paper aims to characterize a 130 nm CMOS power amplifier (PA) with modulated signals, using a well know communication standard, IEEE 802.11ax, the highest power mode was tested. The total Error Vector Manitude (EVM) calculated for 15.00 dBm mean output power (Pout) is 5.60% and for 18.44 dBm Pout is 16.18%, the Power Added Efficiency (PAE) at each point respectively is 18.49% and 25.40% and the large signal gain is 10.59 dB and 8.98 dB. The *loadpull* results were compiled with two values of Pout, 15.00 dBm and 18.44 dBm. The loadpull impedance (Zloadpull) which results in the best EVM were for 85.05 + j83.40 Ω and 27.64 + j62.30 Ω, for each Pout respectively. With these Zloadpull connected, the EVM, the PAE and the large signal gain (GdB) were tested for each Pout. For 15 dBm Pout, the EVM measured is 4.44%, the PAE is 6.95% and GdB is 7.26 dB, and for 18.44 dBm Pout, the EVM measured is 9.56%, the PAE is 10.29% and GdB is 6.45 dB.**

keywords—Power amplifier, IEEE802.11ax, radio-frequency, modulated signals.

I. Introduction

In wireless communications, the power amplifier (PA) is one of the most important circuits in the transmission. It is the component connected directly to the antenna, and so, it is the last circuit that the signal encounters before being transmitted [1]. The PA is responsible for adding power to small amplitude signals, so that they can be transmitted over longer distances or with a small loss of information; for that to happen, the amplifier cannot add significant distortions to the signal. Also, it must be as efficient as possible, since it is the circuit which uses the most amount of power in the transceiver radiofrequency frontend [2].

This paper details results acquired from a previously designed multimode stacked PA [3]. The amplifier was developed using 130 nm CMOS, to operate at 2.4 GHz, and has 4 different operating modes, depending on how many transistors are operating as switches or amplifiers.

The objective of this paper is to evaluate the linearity and the efficiency of the amplifier with two known metrics, the power added efficiency (PAE) and the Error Vector Magnitude (EVM). To follow, is a study of the behavior of the output impedance matching circuit in relation to the EVM of the PA.

II. Power Amplifier

The power amplifier designed in [3], represented in fig. 1, is a stacked PA composed by 4 thick oxide NMOS MOSFETs. As the number of transistors rises, a higher supply voltage can be used, as the voltage drop in each transistor is divided by the number of transistors [4] – [6], making it that the breakdown voltage of each one is not surpassed. Each transistor can be biased to work either as a switch or an amplifier, it is possible, then, to create 4 different modes of operation for this circuit, depending on which transistors are working on each configuration. As the number of amplifiers rises, the gain of the overall circuit increases as well, with the drawback of consuming more DC power, usually resulting in less efficiency. Also, with 4 stacked

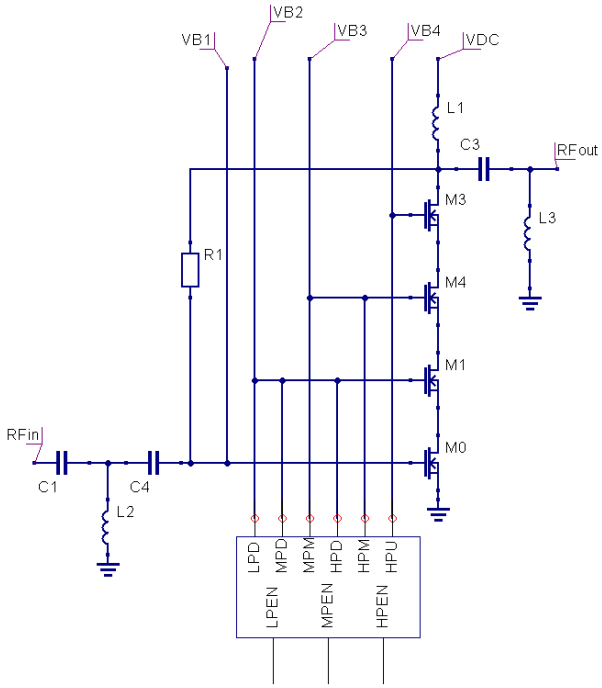

Fig. 1 – Proposed power amplifier

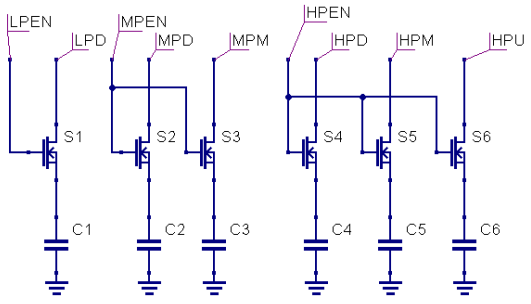

Fig. 2 – Capacitor bank circuit

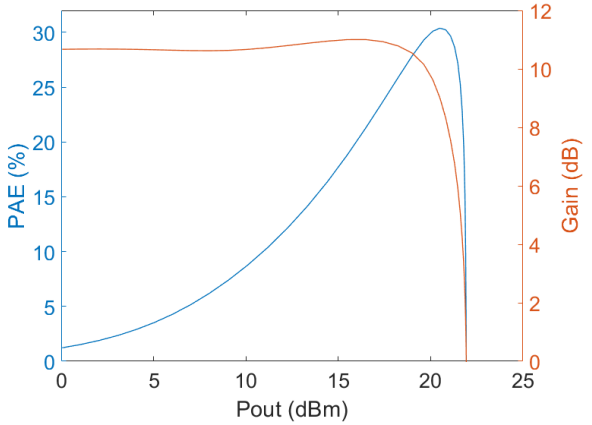

Fig. 3 – Gain (dB) and PAE (%) x Pout (dBm)

transistors, the total phase rotation at the drain of M3 is minimal, and the output power of the amplifier is close to the theoretical total output power [7].

Regarding the dimension of the components, M0-M3 have a total width of 1.2 mm (60 µm per finger), channel length of 240 nm, 20 fingers and double multiplicity. The passive component values of the main circuit are: C1: 303.46 pF; C4: 900 fF; C3: 1.9 pF; L1: 1.8 nH: L2: 4.25 nH and R1: 3.44 kΩ. The transistors from the capacitor bank have a total width of 200 µm (10 µm per finger), channel length of 240 nm, 20 fingers and multiplicity of one, these result in a drain-source capacitance of 50.8 fF and a drain source resistance of 5.25 Ω. The values of the capacitors are: C1: 1 pF; C2: 1.3 pF; C3: 1 pF; C4: 2.9 pF; C5: 2 pF and C6: 800 fF.

Connected directly to the input of the amplifier core is the input matching circuit (IMC) and to the output is the output matching circuit (OMC), which was designed for the highest linearity, maximizing the 1 dB gain compression point when connected to a 50 Ω load. The biasing of each transistor is made using DC inputs on ports VB1 to VB4, as well as LPEN, MPEN and HPEN, where the 3 latter are used to switch the capacitor from the bank capacitor circuit, shown in fig. 2.

The circuit works with four operating modes, and each mode requires a specific DC bias voltage, as well as voltage in each of the DC input pins, the description of the mode is

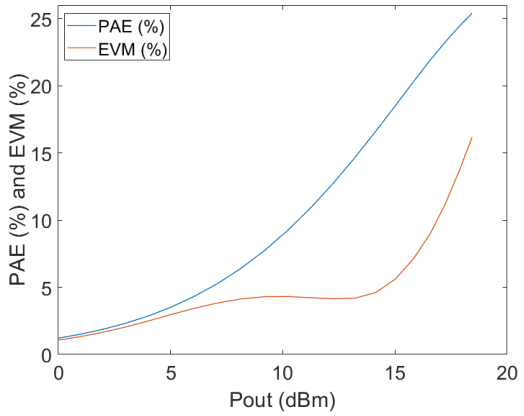

Fig. 4 – EVM (%) and PAE (%) x Pout (dBm)

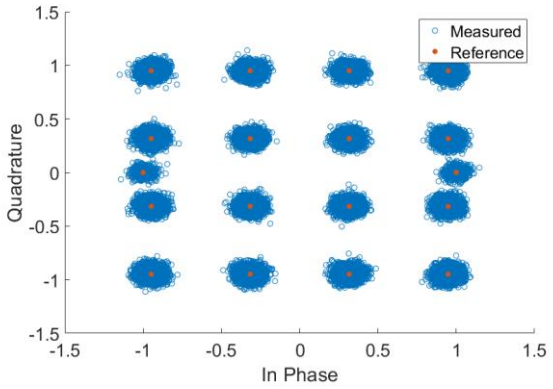

Fig. 5 - Constellation diagram at Pout = 15.00 dBm

given as N4SXAY, where X is the number of switches in the circuit and Y is the number of amplifiers.

III. Results and Discussion

All the simulations were done in Cadence *Spectre* RF [8], in the schematic level. All the metrics mentioned before were determined using 50 Ω input and output impedances. For the biasing, 8 DC fonts were used in total, one for powering the circuit, 4 for the transistors, and 3 to digitally select the capacitors in the capacitor bank.

The circuit was simulated in its highest power mode, the N4S0A4 mode, which is the one that requires the highest DC power voltage, as all the transistors in the circuit are working as amplifiers.

A. *Large signal continuous-wave simulation*

The harmonic balance simulation was configured to an average input power (Pin) range of -15 dBm to 20 dBm.

Figure 3 shows the large signal gain of the amplifier in dB (GdB) and the PAE, both in relation to the average output power measured in the load (Pout). The maximum large signal gain verified from the graph is 11.00 dB. The 1 dB gain compression point (OCP1dB), which is, the Pout of the PA when the gain falls 1 dB from the maximum is 19.63 dBm. The PAE at OCP1dB is 29.30%, and the maximum PAE of the amplifier is 30.38%.

B. *Modulated signals simulation*

For the second set of results, an envelope simulation with modulated signals was configured, which determines the

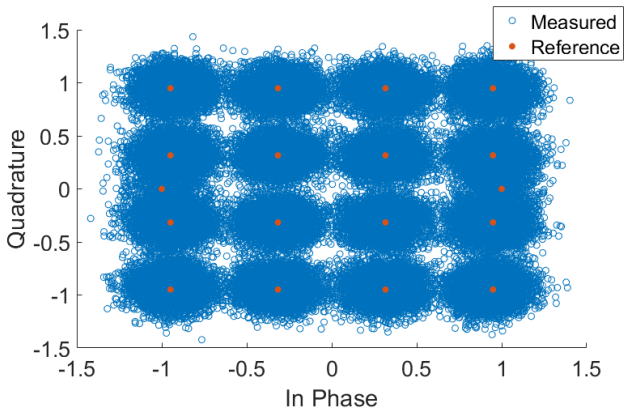

Fig. 6 – Constellation diagram at Pout = 18.44 dBm

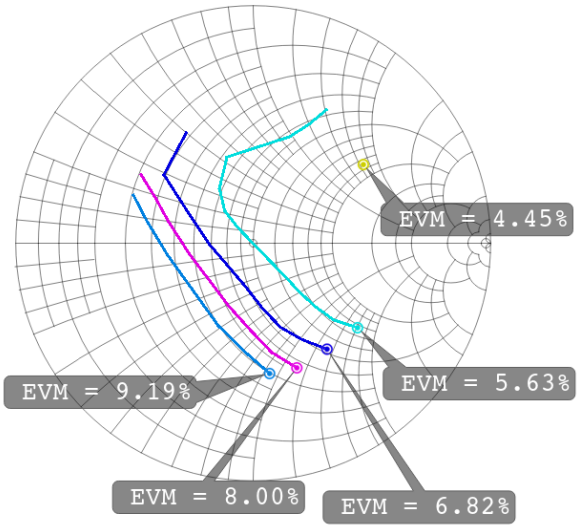

Fig. 7 – Loadpull contours of constant EVM at Pout = 15.00 dBm

EVM of the circuit. The simulation was configured with the communication standard IEEE 802.11ax. The input signals have a carrier frequency of 2.4 GHz, a 16QAM modulation and occupy a bandwidth of 80 MHz.

The first step was to determine the EVM at different mean output power levels, for this, it was compiled a graph that shows the EVM and PAE of the PA in relation to Pout, it can be seen in figure 4. This behavior agrees with the one observed in figure 3, where some gain expansion is observed before compression and saturation. After, two values of Pout were chosen to measure the constellation diagrams at this operating power, the reference constellation and the measured constellation when the PA is outputting a Pout of 15.00 dBm and 18.44 dBm can be seen in figures 5 and 6. The total EVM calculated from the graph for 15.00 dBm and 18.44 dBm respectively are 5.60% and 16.18%, the average PAE calculated at those Pout are, respectively, 18.49% and 25.40%. The mean large signal gain at those Pout are 10.59 dB and 8.98 dB.

Using the same configurations, the *loadpull* simulation was done, to create curves of constant EVM using the Smith chart. With those curves, the best *loadpull* impedance can determined, that impedance connected to the load will result in the smallest EVM possible measured at the output. The

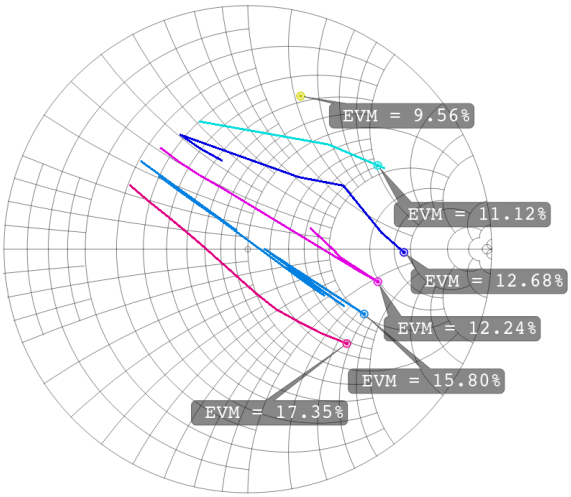

Fig. 8 – Loadpull contours of constant EVM at Pout = 18.44 dBm

Smith plane with the constant EVM contours, for both input powers, can be seen at figure 7 and 8, on the graph, the value of the EVM at each trace is shown in both graphs.

From the Smith plane it can be seen that the lowest EVM possible with this configuration is 4.45%, for 15.00 dBm Pout, and 9.56%, for 18.44 dBm Pout. The *loadpull* impedance (Zloadpull) for the two values of Pout were different, for 15.00 dBm it is 85.05 + j83.40 Ω and for 18.44 dBm it is 27.64 + j62.30 Ω.

To test these results, the load impedance (Zload) connected to the output of the PA for both Pouts, each with its respective value of Zloadpull. After Zload was changed, the EVM was measured, similarly with figures 6 and 7. Figure 9 shows the reference 16QAM constellation, and the measured EVM of the signals at the 85.05 + j83.40 Ω Zload, with a Pout of 15.00 dBm. With these parameters, the PAE is 6.95% and GdB is 7.26 dB. Figure 10 shows the same reference constellation as before and the EVM of the signal at the 27.64 + j62.30 Ω Zload, with a Pout of 18.44 dBm. With the operating parameters the PAE is 10.29% and the large signal gain is 6.45 dB.

From these results it can be seen that changing the load impedance the EVM can reduce at both power levels, as can be seen in figure 11. The downside is that the efficiency of the PA and the mean gain lower in both cases, as can be seen in figure 12, which presents the PAE of the PA for all three load impedances, in relation to the input power of the PA. Table 1 compiles all the results discussed above.

IV. Conclusion

The main purpose of this work was to characterize the PA presented and described in it, with the IEEE 802.11ax communication standard. The work presents several metrics that determine some of the main characteristics desired in a power amplifier, such as efficiency, represented in this work by the PAE.

The results presented in this work show that the PA presents several good metrics, in relation to efficiency and linearity. With the EVM metric is in mind, when Pout is close to the area with the maximum gain, a low EVM can be observed, when Pout increases the EVM also increases drastically. Changing the OMC network, better results of EVM can be achieved, as can be seen with the *loadpull* curves, with a loss in the efficiency and the gain of the circuit.

The next step in this work is to design an OMC network to maximize the EVM measured at the output of the circuit. For this purpose, one can use an impedance matching calculator to select the best topology and values for the components which make part of the circuit. It is important that the new OMC does not hurt too much the rest of the metrics measured on the PA.

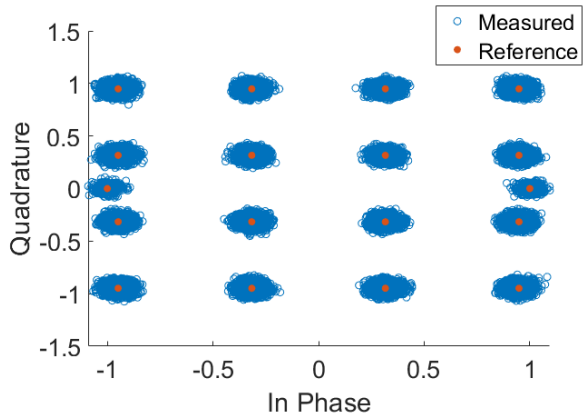

Fig. 9 – Constellation diagram at Pout = 15.00 dBm and Zload of 85.05 + j83.40 Ω.

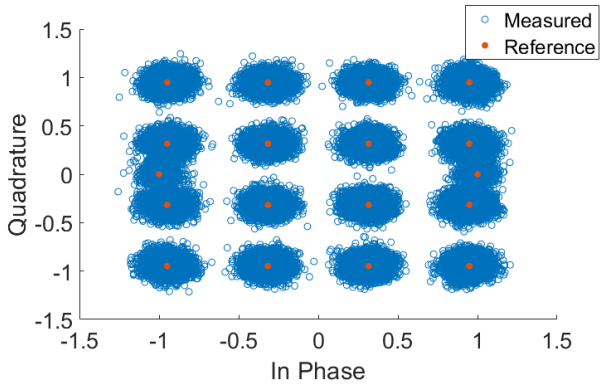

Fig. 10 – Constellation diagram at Pout = 18.44 dBm and Zload of 27.64 + j62.30 Ω.

TABLE I. COMPILED RESULTS OF THE PAPER

Mean output power (dBm)	Before loadpull simulation (50 Ω load)			After loadpull simulations (85.05 + j83.40 Ω and 27.64 + j62.30 Ω loads.)		
	EVM (%)	PAE (%)	Gain (dB)	EVM (%)	PAE (%)	Gain (dB)
15.00	5.60	18.49	10.59	4.45	6.95	7.26
18.44	16.18	25.40	8.98	9.56	10.29	6.45

V. REFERENCES

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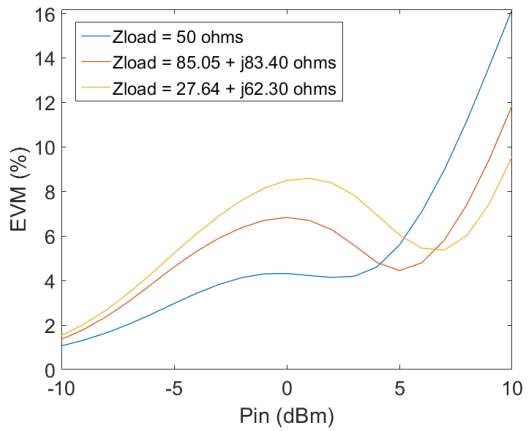

Fig. 11 – EVM (%) x Pin (dBm) for all load impedances

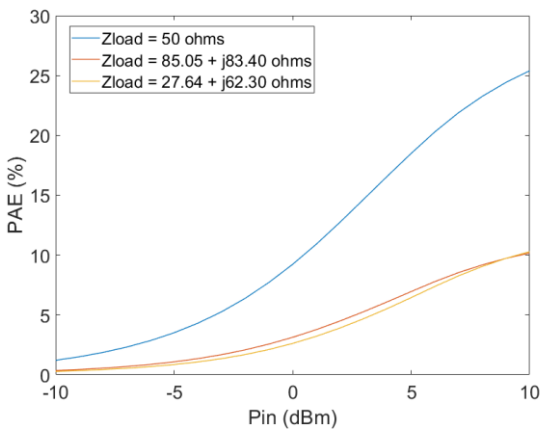

Fig. 12 – PAE (%) x Pin (dBm) for all load impedances