Stability and Linearity Improvement in a Multi-Mode CMOS Power Amplifier

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***Abstract*—This work presents the results obtained by applying stability and linearity improvement techniques in a multi-mode power amplifier (PA) with four distinct modes of operation. It consists of a differential CMOS amplifier in 130 nm technology that uses cascode topology and has two main stages, a gain, and a power stage. The original PA presents unconditional stability in schematic simulations, but when tested alone, both the gain and power stages did not show unconditional stability, which also led to potential instability for the complete PA in post-layout simulations. Therefore, in order to make the individual stages unconditionally stable, the original circuits were modified. Thus, crossed capacitors were added in the gain stage, and an RC network was modified in the power stage. With this, the modified circuit had an improvement in overall stability with a slightly decreased but more constant gain value, which in the original circuit ranged from 30.3 dB to 31.7 dB, and now ranges from 28.6 dB to 28.8 dB. In addition, there was little impact on the power-added efficiency (PAE). Also, the OCP_{1dB} improved, where, in the original circuit, it ranged from 20.6 dBm to 25.5 dBm, and now ranges from 20.9 dBm to 25.6 dBm.**

***Index Terms*—Power amplifier, Stability, Multi-mode**

I. Introduction

The number of battery-powered mobile devices that use wireless communication increases every day. For this type of communication to be possible these devices have one system in common, the power amplifier (PA). This system is responsible for amplifying small signals to the required power level before transmission. As a result, this system consumes a large amount of power, which comes from the battery. Considering that mobile devices constantly vary their distance from the receiver, as well as their data requirements, the same output power levels are not always required.

As presented in [1], using a multimode PA can help save battery power by using different modes of operation. These modes have higher or lower power consumption depending on the required output power level.

The PA presented in [2] has seven different modes of operation. In this circuit, the modes are controlled by a 3-bit digital signal that turns on and off transistors with different widths thus generating different power levels.

Other examples of multi-mode PAs can be seen in [3], [4]. These PAs also have cells that can be turned on and off by digital signals.

The circuit proposed by [1] consists of a differential multi-mode PA using cascode topology in 130 nm CMOS technology. This PA has two stages, a gain stage, and a power stage. This circuit can switch between four different modes that vary its output power and, by doing that, also vary its power consumption. It has lower consumption for the mode with lower output power, and higher consumption for the mode with higher output power. In addition, this circuit aims to have a low gain variation between the four modes of operation.

Therefore, the circuit proposed by [1] shows great results and unconditional stability in the schematic-level simulations. However, after post-layout simulations, it was found that the circuit no longer exhibited unconditional stability.

With this, this paper presents the results obtained when applying stability and linearity improvement techniques in this circuit, in order to improve its overall stability in post-layout simulations, and aiming to make the circuit also unconditionally stable in this stage. To achieve this, modifications were made to the schematics of the gain and the power stages, since when tested alone, both these stages did not present unconditional stability for the four modes of operation. Therefore, the main objective of this work is to make these two stages unconditionally stable without worsening other important metrics for the operation of the PA. In section II, the original circuit will be presented, as well as the modifications made in its two stages. Section III presents, through simulation results, the impacts of these modifications.

II. Circuit and Modifications

A. Original circuit

The circuit proposed by [1] consists of a differential multi-mode power amplifier with cascode topology, designed to operate at a frequency of 2.45 GHz. The circuit is composed of two stages, the gain stage, responsible for increasing the amplifier gain, and the power stage, responsible for delivering a high output power. All the transistors used are thick oxide and have a channel length of 240 nm. The width of the transistors is defined by the number of fingers. 60 μm fingers were used for the gain stage and 50 μm fingers for the power stage. There are also 3 impedance matching networks, in the input, between the two stages, and in the output.

TABLE I
OPERATION MODES.

Mode	En1A	En2A	En2B	En2C
A	1	0	1	1
B	0	1	0	1
C	0	1	1	0
D	0	1	1	1

In addition, both stages have transistors that can be switched on and off through digital signals applied to pin En1A, of the gain stage, and pins En2A, En2B, and En2C of the power stage, thus generating the circuit's four modes of operation. The combinations that generate these modes are shown in Table I. Mode A has the lowest output power and lowest power consumption, and mode D has the highest output power and highest power consumption. Since the only enable signal present in the gain stage is the En1A signal, this stage effectively has only two modes of operation.

The gain stage, shown in [1, Fig.1], is composed of a differential cascode cell made of two common source transistors with effective width W of 360 μm, and four common gate transistors with effective widths of 240 μm and 120 μm. In this case, one of the common gate transistors is always activated, and the second transistor is only activated when the transistor that has the biggest width of the power stage is switched off, that is, when operation mode A is selected. This helps to compensate for the decrease in gain caused by the lack of this transistor.

The power stage, shown in [1, Fig.2], is composed of a differential cascode cell made of two common source transistors with effective width W of 2.1 mm, and six common gate transistors with effective widths of 300 μm, 600 μm and 1200 μm. In addition, an RC feedback network is used to improve stability. In this network the resistor R has a resistance of 390 Ω, and the capacitor C has a capacitance of 743 fF.

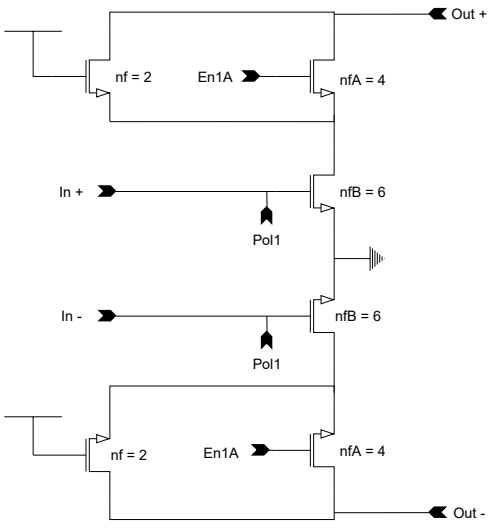

Fig. 1. Gain stage schematic.

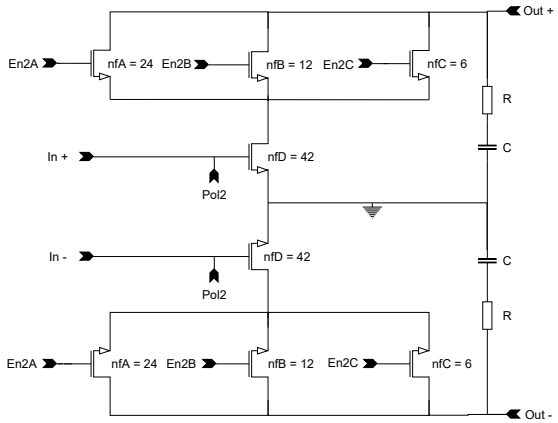

Fig. 2. Power stage schematic.

B. Modifications

Analyzing ways to increase the circuit's overall stability, several simulations of the μ parameter were performed. This parameter shows if the circuit is unconditionally stable or not. When simulated independently, both gain and power stage contained frequency ranges in which the μ parameter showed values smaller than one, that is, not presenting unconditional stability. Thus, it was decided to modify these two stages, so they would also present unconditional stability, improving the circuit's overall stability.

Starting with the gain stage, when simulated alone, this stage only has two effective modes of operation. The first one happens when mode A of the PA is used, that is, when the applied voltage on the En1A pin is equal to 2.7 V. The second one happens when modes B, C, and D are used, that is, when the voltage in the En1A pin is equal to 0 V. With this, using a supply voltage, and signal activation voltage of the pin En1A, of 2.7 V, and simulating the circuit in a frequency range that varies from 100 kHz up to 10 GHz, the B, C, and D modes of this stage presented μ value lower than one in the frequency range that goes from approximately 2.8 GHz up to 6.5 GHz. This result is shown in Fig.3. Therefore, to increase stability and make the μ parameter greater than one for the entire simulated frequency range, without much degradation in the PA metrics, cross capacitors were added between the drains and sources of the common source transistors. Fig.4 shows the new circuit topology. After optimizations the capacitance was defined as 83 fF. These capacitors are of the MIM type.

Regarding the power stage, when simulated alone, also in the frequency range of 100 kHz up to 10 GHz, with a supply voltage of 3.2 V and activation voltage of the En2A, En2B, and En2C signals equal to 2.7 V, it was observed that, as shown in Fig.5, all operation modes showed a value of μ lower than one in the frequency range between 2.2 GHz up to 6.4 GHz. With this, also aiming to obtain a stability improvement in the circuit, and not degrade too much the other metrics, changes were made in the values of the RC feedback network already present in the circuit, so it was not necessary to modify the

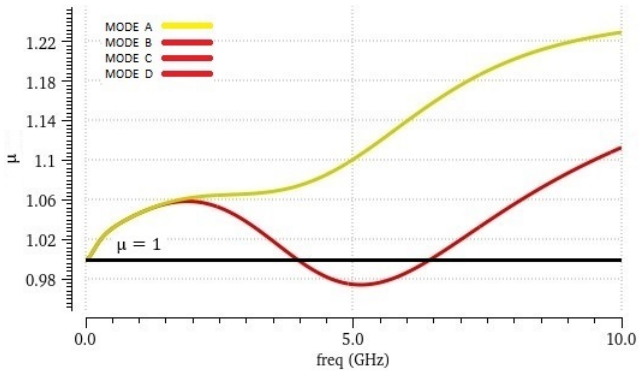

Fig. 3. Gain stage original μ parameter graph.

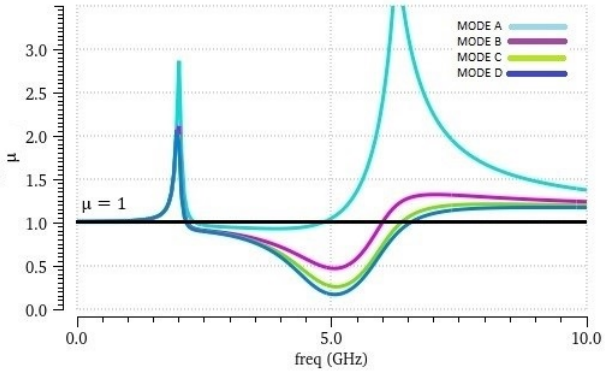

Fig. 5. Power stage original μ parameter graph.

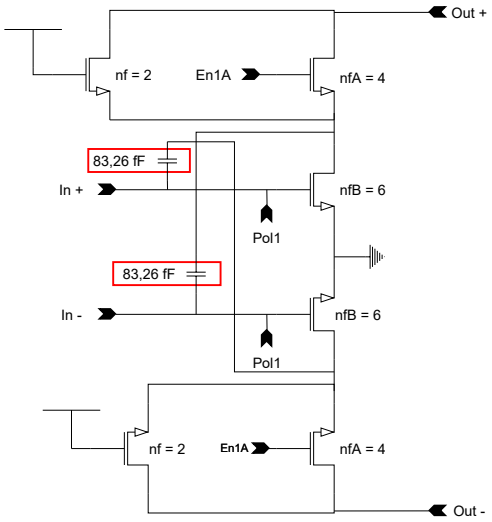

Fig. 4. Modified gain stage schematic.

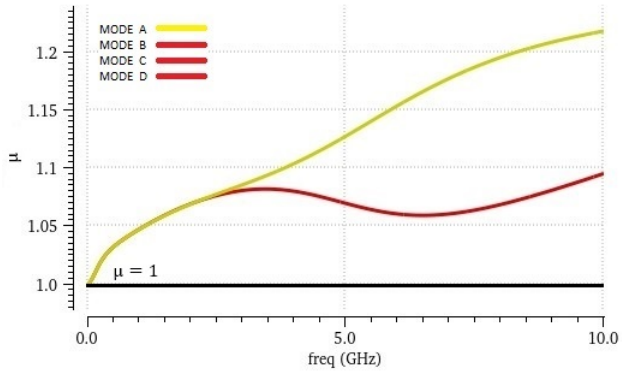

Fig. 6. Modified gain stage μ parameter graph.

circuit topology. This way, after simulations resistors with 142.07 Ω and dual MIM type capacitors with a capacitance of 8.12 pF were used.

III. Simulation Results

In this section, the impacts of the changes made in the circuit will be presented through simulations. All simulations were performed using the software Cadence Spectre RF [5]. For both stages, the simulations were performed keeping the same frequency range and voltage values already mentioned in the previous section.

Fig.6 shows the simulation result of the μ parameter obtained with the new gain stage circuit. This graph shows that all modes are now unconditionally stable.

Fig.7 shows the result of the simulation of the μ parameter performed with the new circuit of the power stage. Like the new gain stage circuit, now this stage also presents unconditional for all modes of operation.

Fig.8 shows the result of the simulation of the gain versus the output power for the modified PA. This graph clearly shows the differences in gain and OCP_{1dB} between each mode of operation.

Table II compares the original complete circuit proposed by [1], and the modified circuit presented in this work. With this, it is possible to notice that the changes made in the circuit, besides increasing its stability, also increased linearity since the OCP_{1dB} values have improved for all modes of operation. Furthermore, these modifications brought little impact on other metrics such as power-added efficiency (PAE), which now, at OCP_{1dB}, presents smaller values when using modes A and D, and greater values when using modes B and C. The gain despite having its value decreased, now presents a smaller variation between modes, reducing possible distortions.

Finally, Table III shows a comparison between this work and other PAs found in the literature. One of the differences of the PA presented in this work is that the variation in gain between modes of operation is really small. It also presents high gain and OCP_{1dB} values.

IV. Conclusions and Future Work

This paper presented the modifications performed on a multi-mode PA in order to make its individual stages unconditionally stable. With this, the modifications performed proved to be effective in increasing the stability and linearity of the circuit without significantly affecting the other metrics

TABLE II
ORIGINAL AND MODIFIED CIRCUIT COMPARISON

Mode	OCP_{1dB} (dBm) [1]	OCP_{1dB} (dBm) This work	Gain (dB) [1]	Gain (dB) This work	Maximum PAE (%) [1]	Maximum PAE (%) This work	PAE at OCP_{1dB} (%) [1]	PAE at OCP_{1dB} (%) This work
A	20.6	20.9	30.3	28.6	14.4	13.4	9.3	9.0
B	22.2	22.8	29.6	28.4	20.8	19.4	11.5	12.0
C	23.6	24.1	30.2	28.8	23.6	22.0	13.2	13.7
D	25.5	25.6	31.7	28.8	26.6	24.1	14.6	13.8

Schematic simulation results.

TABLE III
COMPARISON TO THE STATE-OF-THE-ART

References	[1]	[2]	[3]	[4]	This work
Technology	130 nm	130 nm	130 nm	65 nm	130 nm
Frequency (GHz	2.45	2.4	2.4	2.5	2.45
Number of modes	4	7	6	4	4
Gain (dB)	31 - 32	13 - 21	22 - 31	16 - 24	29[2]
OCP_{1dB} **(dBm)**	21 - 25	6.0 - 18	14	17 - 26	21 - 26[2]
PAE at OCP_{1dB} **(%)**	8 - 12	2.0 - 17	13 - 15[3]	5.0 - 12	9 - 14[2]

1 - Post-layout simulation result, 2 - Schematic simulation result, 3 - Estimated Values.

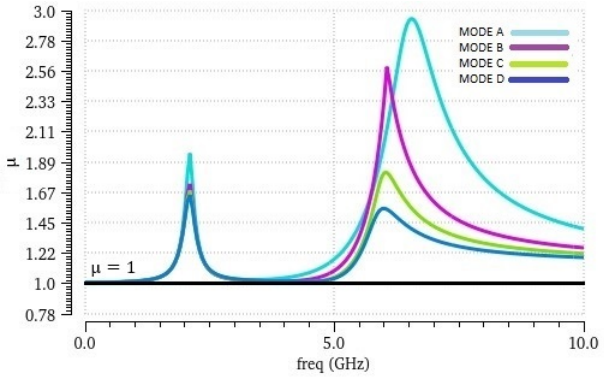

Fig. 7. Modified power stage μ parameter graph.

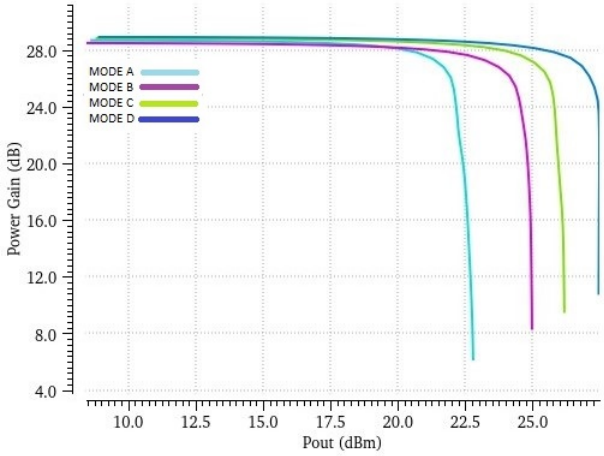

Fig. 8. Modified amplifier gain versus output power graph.

of the PA. In addition, the decrease obtained in gain variation between modes is another very positive point.

In a future work, the design of the new layout will be carried out in order to find out whether the modifications presented in this paper were able to make the circuit unconditionally stable in post-layout simulations.

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