# Adaptive Biasing Circuitry for a CMOS Power Amplifier

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***Abstract*—This work introduces an adaptive network for a $CMOS$ power amplifier. The circuit generates logical signals, determined by the radiofrequency signal input power. Applying these outputs to a amplifier, it's possible to configure the amplification level. The controller consists of three subcircuits: an envelope detector, which is tracks the power levels of the modulated input signal; a quantization stage, composed by comparators and activated when the input power reaches an voltage threshold and a logic circuit which receives the quantized signal and converts it into binary logic output. This work is developed for a amplifier with 4 modes of operation and three digital inputs. After a simulation, the four logical sequences corresponding to each operation mode of the amplifier were obtained. The first digital transition occurs when the input voltage reaches $0.4\,\mathrm{V}$. The second transition occurs when the input reaches $1.075\,\mathrm{V}$. And the last transition occurs when the voltage reaches $2.2\,\mathrm{V}$.**

***Index Terms*—Power amplifier, adaptive polarization, radiofrequency.**

## I. Introduction

With the increasing demand for wireless communications, such as the new 5G networks, the need for power amplifiers (PA) that offer high energy efficiency, high linearity, and coverage across a wide frequency spectrum becomes crucial. Due to function at the transmitter, a PA consumes a significant amount of power. In addition to amplification, it also needs to maintain a good level of linearity between the input and output signals. So, due to the requirements for efficiency and the need for linearity, a compelling solution is using reconfigurable PAs.

This type of amplifier has the ability to change the operation mode, adapting to meet the required power for signal transmission, as in the PA proposed by [1]. Depending on the magnitude of the input radiofrequency (RF) signal power, the amplifier will be configured in a specific mode of operation that consumes more or less power. The relationship between the input signal and power consumption depends on the characteristics of the PA.

However, these operating states need to be controlled based on the power of the RF transmission signal. Therefore, it is interesting to implement a circuit alongside the PA that performs mode control.

To develop this controller was used, as prototype, the PA designed by [1]. The author proposes 4 operation modes named: A, B, C, and D. The PA is based on $130\,\mathrm{nm}$ $CMOS$ technology with central frequency of $2.45\,\mathrm{GHz}$. To ensure better stability and linearity, a second study conducted by [2] improved the circuit adding capacitors for stabilization. The PA consists of two stages: a direct gain stage and a power gain stage, both of which can be controlled by the digital inputs $E_N2A$, $E_N2B$, and $E_N2C$, this same nomenclature will be used to refer to controller digital outputs. The table I shows the truth table between PA digital inputs and the comparators outputs. It will be detailed better on II-D.

In short, this work presents an analog-to-digital control circuit for programmable amplifiers and analyzes its behavior based on the variation of the input signal power.

## II. Control System Circuit

### A. Overview

The circuit designed for PA control, shown in Fig. 1, is divided into three subcircuits. The first one is an envelope detector that, upon receiving a modulated high-frequency signal, provides the envelope shape of the demodulated signal at the output. Next, there is a quantization stage consisting of high-speed comparators. These comparators receive the demodulated signal and toggle their output state based on the comparison between the input magnitude and pre-established reference voltages. Finally, the logic circuit receives the comparator states and determines the binary sequence at the output that will be applied to the PA. The channel length of all transistor is $240\,\mathrm{nm}$. Adding it, the biasing voltage $Vdd$ is $3.2\,\mathrm{V}$ and $VddLogAmp$ and $Vbias$ are equal to $2.7\,\mathrm{V}$.

### B. Envelope Detector

The envelope detector consists of three additional sub-elements: the detector element, the differential logarithmic amplification stage, and the differential to single-ended output

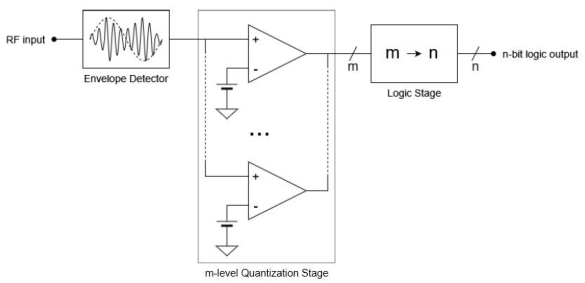


Fig. 1. Full Control Circuit Schematic.

converter. The envelope detector, being the most complex element, as it needs to ensure certain premises such as high sensitivity to high-frequency signals with very low magnitude, while also being efficient in terms of power consumption. is divided into three subcircuits. In the development of this model, works such as [3], [4], and [5] were analyzed. [3] was particularly interesting due to its suitability for multiple standard operations, while [5] presented a high-performance detector. It is shown in Fig. 2 the envelope scheme.

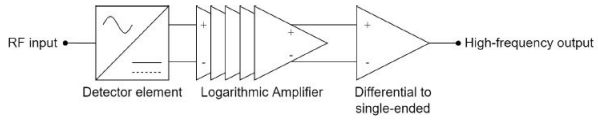


Fig. 2. Envelope Detector Schematic.

*1) Detector Element:* The detection element is of the standard type, allowing it to track low-level signals at the input but not capable of amplifying them. The circuit consists of a differential pair composed of $NMOS$ transistors and a current mirror with $PMOS$ transistors for biasing the pair. Additionally, capacitors are connected in parallel to the drain and source terminals of the $NMOS$ transistors to improve circuit stability. Lastly, impedance matching at the input reduces signal losses. In summary, when the positive component of the modulated signal is applied to the input of the detector, a differential signal proportional to the input magnitude will be generated at its output, same concept shown in [4]. Above is shown in Fig. 3 the circuit developed.

*2) Differential Logarithmic Amplifier:* Although the detection component effectively tracks low-power signals, the magnitude at the output of the differential pair is too small to be directly quantified by the logic conversion stage. Therefore, signal amplification is required. A logarithmic amplifier circuit with five gain stages is proposed for this task, as shown in Figs. 4 and 5. The circuit concept was based on references [6] and [7], which present differential $CMOS$ logarithmic amplifiers. The figure 4 presents the input of the amplifier circuit. The signal is received at the $V_{IN}+$ e $V_{IN}-$ inputs and transmitted through $V_{OUT}+_n$ and $V_{OUT}-_n$ to the first of the five series circuits in the amplification stage. The schematic diagrams of the circuits are presented in Fig. 5. The number of stages allows the amplifier output to follow the power curve

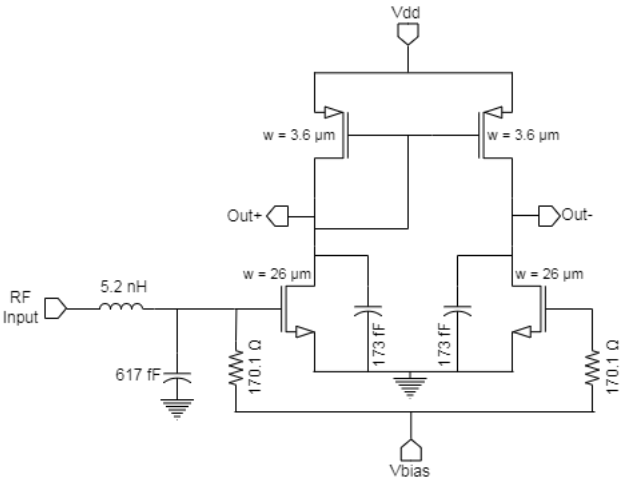


Fig. 3. Detector Element Schematic.

proportionally rather than the voltage curve, as commented in [7]. Another advantage of the circuit is its precision in tracking small variations in input power and its contribution to reducing signal distortion. The latter is a direct consequence of using the logarithmic amplifier, as it draws less power from the input signal, reducing distortion on the PA control circuitry.

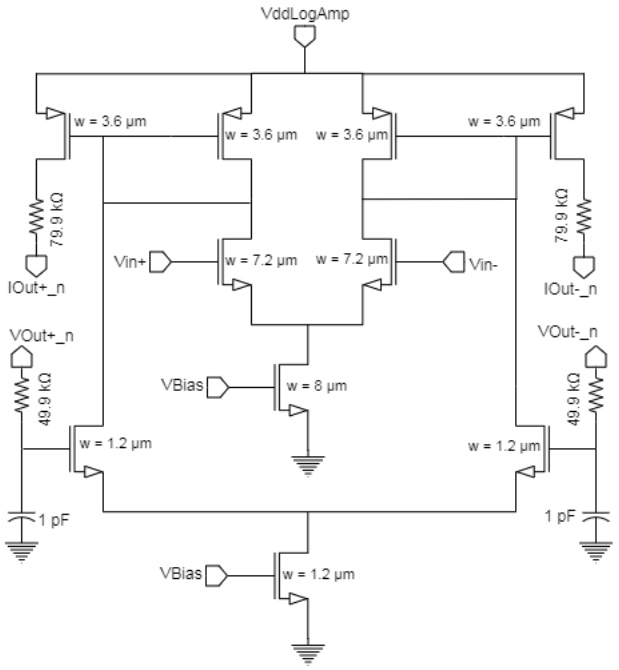


Fig. 4. Input Schematic of Differential Logarithmic Amplifier.

*3) Differential To Single Ended Converter:* Finally, after amplifying the detected signal, it needs to be converted back to a single-ended signal. This third component based on the design principles described in [8]. The circuit is shown in Fig.6. The result of the conversion is an amplified signal, with behavior directly proportional to the power of the input RF signal of the amplifier. A detailed design of an converter can

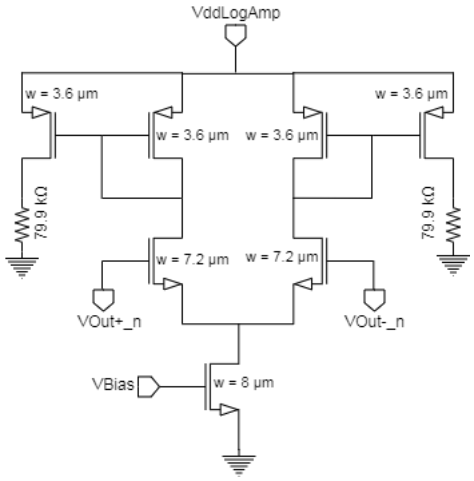


Fig. 5. Amplifier Schematic of Differential Logarithmic Amplifier.

be obtained in [8].

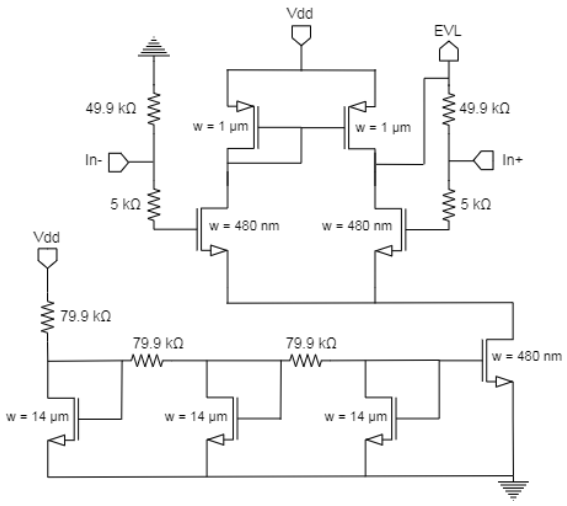


Fig. 6. Differential To Single Ended Converter Schematic.

### C. Quantization Stage Circuit

As the project aims to program logical outputs based on the power of a modulated RF signal, the last stage is the implementation of the signal quantization circuit. The proposed circuit is easily adaptable depending on the number of operating modes of the PA. In this project, the concept of $m+1$ possibilities of modes is used, with the number of comparators in the quantization stage equal to $m$. Each comparator has an adjustable reference voltage $V_X$ based on the desired behavior of the PA. If the goal is to have a PA with good efficiency, even if it results in distortions at signal peaks, the $V_X$ thresholds should be higher. On the other hand, if the focus is on linearity, even if it leads to increased power consumption, lower values for $V_X$ are appropriate. In addition to quantizing the magnitude of the RF signal, modern modulations can generate 80 million symbols per second, requiring high-speed comparators to keep up with the received signal from the detector.

### D. Logic State Circuit

Finally, the final stage of the controller circuit is the conversion of power quantization into logical signals that will control the PA. In this stage, it is necessary to define the quantization levels and the number of amplifier operation modes. With this information, a truth table is created that relates the comparator outputs to the digital outputs, and finally, the logical circuit with NAND gates is developed.

Since the target PA from [1] has 4 modes of operation, the number of comparators will be 3, given by $m + 1$. The comparators share a common input, the signal from the envelope detector $EVL$, and each has its adjustable reference voltage, $V_X$. Their outputs are $CR_A$, $CR_B$, and $CR_C$, which result from comparing the inputs. When $EVL$ is greater than $V_X$, the output is activated; otherwise, it is deactivated. Based on the PA from [1], a truth table was created between the comparator outputs $CR_A$, $CR_B$, and $CR_C$ and the digital inputs of the PA, $E_N2A$, $E_N2B$, and $E_N2C$. Furthermore, it was determined that the terminals $CR_X$ should be activated sequentially. Table I below presents the relationship between the inputs $P_X$ and the outputs $E_N2X$.

TABLE I
TRUTH TABLE TO $CR_X$ AND $E_N2X$

| Operation Mode | Input Signal | | | Output Signal | | |
|---|---|---|---|---|---|---|
| | $CR_A$ | $CR_B$ | $CR_C$ | $E_N2A$ | $E_N2B$ | $E_N2C$ |
| **A** | ***0*** | ***0*** | ***0*** | ***0*** | ***1*** | ***1*** |
| **B** | ***1*** | ***0*** | ***0*** | ***1*** | ***0*** | ***1*** |
| **C** | ***1*** | ***1*** | ***0*** | ***1*** | ***1*** | ***0*** |
| **D** | ***1*** | ***1*** | ***1*** | ***1*** | ***1*** | ***1*** |

Using the Table I above, the logical expressions for the PA designed by [1] were determined as follows:

$$E_N2A = CR_A \tag{1}$$

$$E_N2B = \overline{CR_A} + CR_B = \overline{\overline{\overline{CR_A} + CR_B}} = \overline{CR_A \cdot \overline{CR_B}} \tag{2}$$

$$E_N2C = \overline{CR_B} + CR_C = \overline{\overline{\overline{CR_B} + CR_C}} = \overline{CR_B \cdot \overline{CR_C}} \tag{3}$$

Knowing these expressions, the logical circuit schematic for the PA was created. Fig. 7 shows this scheme.

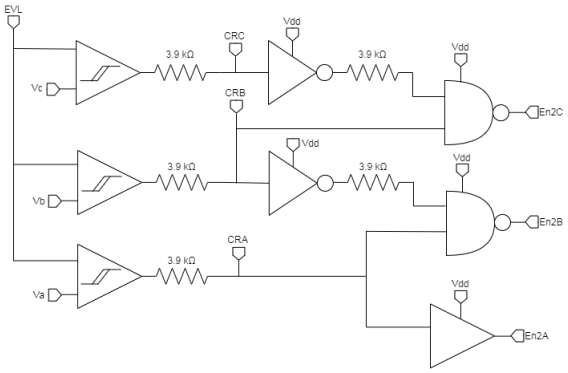


Fig. 7. Logic Circuit Schematic.

## III. Simulation Results

After conclude the controller, a Harmonic Balance simulation was performed, using Cadence Virtuso software, applying a sinusoidal signal at the input of the controller. The results obtained are shown in Fig. 8, illustrating the behavior of the comparators, and Fig. 9, presenting the digital logic outputs.

Fig. 8 depicts the output behavior of the three comparators. The importance of this result lies in verifying that the transitions of the $CR_X$ outputs occur precisely when the value of $EVL$ reaches the threshold voltage.

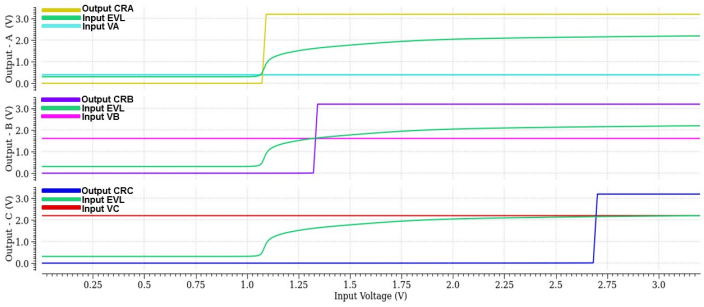


Fig. 8. Comparator Simulation Results.

In the first comparator, the threshold voltage $V_X$ was set to $0.4\,\mathrm{V}$. When the input signal of the comparator, $EVL$, reached the minimum value of $0.4\,\mathrm{V}$, the quantized output $CR_A$ is activated, changing its logic state from low to high, near an input voltage of $1.075\,\mathrm{V}$. In the second comparator, the threshold voltage $V_X$ was selected as $1.61\,\mathrm{V}$. When the $EVL$ signal reached the minimum value of $1.61\,\mathrm{V}$, the quantized output $CR_B$ is activated, changing its logic state from low to high, near an input voltage of $1.325\,\mathrm{V}$. Finally, in the third comparator, the threshold voltage $V_X$ was set to $2.2\,\mathrm{V}$. As soon as the $EVL$ signal reaches the threshold value, the quantized output $CR_C$ is activated, changing its logic state from low to high, near an input voltage of $2.675\,\mathrm{V}$.

Looking at Fig. 9, it can be observed that the digital outputs exhibit transitions when the threshold voltages $V_X$ are reached. Thus, the controller circuit is behaving as expected according to the logic table Table I.

Regarding the digital inputs, $E_N2A$, $E_N2B$, and $E_N2C$, mentioned above, they initially have the configuration $011$. At the moment when $1.075\,\mathrm{V}$ is reached at the input, the output of first comparator is activated, and the state of the inputs changes to $101$. When the second comparator reaches its threshold at an input voltage of $1.325\,\mathrm{V}$, the state of the digital inputs is again altered to $110$. Finally, with the third comparator activated at an input voltage of $2.675\,\mathrm{V}$, the last possible logical state is obtained at the output of the controller circuit, which is $111$.

## IV. Conclusion

This work presented a proposal for a $CMOS$ PA controller circuit. The main idea of the component is to output a digital sequence, which will configure the operating mode of a $CMOS$ PA, based on the application of the positive part of the modulated high-frequency RF signal to the input of the controller. The binary sequence regarding the operating mode and input RF signal should be adjusted depending on the PA. Analyzing the simulations it can be noted that the controller operates as desired based on the logical behavior. Each of the digital states is being selected as the comparators have their outputs altered when the $EVL$ signal reaches the previously established threshold voltages. For input voltages below $0.4\,\mathrm{V}$, the output remained at $011$. Beyond this threshold, it changed to $101$. When the second threshold, $1.61\,\mathrm{V}$, was reached, the digital output became $110$. Finally, when the third voltage threshold of the last comparator was reached at $2.2\,\mathrm{V}$, the final configuration was $111$. Furthermore, the circuit can be applied together with a PA to evaluate the gain, linearity, and efficiency behaviors with and without the controller.

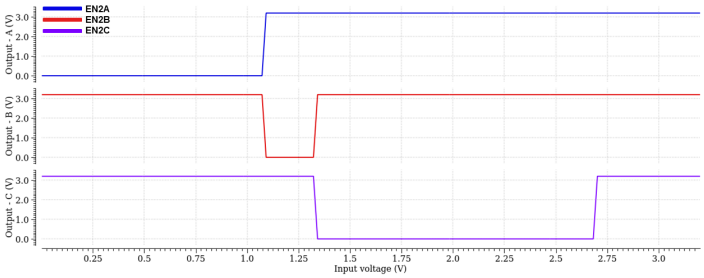


Fig. 9. Digital Output Simulation Result.

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