SBCCI 2021 - 2021 SSCS - CEDA - CASS Brazil Mini-colloquium

8:45 – 9:45
Title: **Hardware Supported Cybersecurity for IoT**
Speaker: **Yier Jin** – University of Florida (USA)
Chair: **José Guntzel** – Chair of the IEEE CEDA Brazil Chapter

Abstract:

Within the past decade, the number of IoT devices introduced in the market has increased dramatically. The total is approaching a staggering 15 billion, meaning that there are currently roughly two connected devices per living human. However, the massive deployment of IoT devices has led to significant security and privacy concerns given that security is often treated as an afterthought for IoT systems. Security issues may come at different levels, from deployment issues that leave devices exposed to the internet with default credentials, to implementation issues where manufacturers incorrectly employ existing protocols or develop proprietary ones for communications that have not been examined for their sanity. While existing cybersecurity and network security solutions can help protect IoT, they often suffer from limited onboard/on-chip resources. To mitigate this problem, researchers have developed multiple solutions based on a top-down (relying on the cloud for IoT data processing and authentication) or a bottom-up (leveraging hardware modifications for efficient cybersecurity protection). In this talk, I will first introduce the emerging security and privacy challenges in the IoT domain. I will then focus on the bottom-up solutions on IoT protection and will present our recent research effort in microarchitecture supported IoT runtime attack detection and device attestation. The developed methods will lead to a design-for-security flow towards trusted IoT and their applications.

Biography:

Yier Jin is the Endowed IoT Term Professor in the Warren B. Nelms Institute for the Connected World and also an Associate Professor in the Department of Electrical and Computer Engineering (ECE) in the University of Florida (UF). Prior to joining UF, he was an assistant professor in the ECE Department at the University of Central Florida (UCF). He received his PhD degree in Electrical Engineering in 2012 from Yale University after he got the B.S. and M.S. degrees in Electrical Engineering from Zhejiang University, China, in 2005 and 2007, respectively. His research focuses on the areas of embedded systems design and security, trusted hardware intellectual property (IP) cores

and hardware-software co-design for modern computing systems. He is currently focusing on the design and security analysis on Internet of Things (IoT) and wearable devices with particular emphasis on information integrity and privacy protection in the IoT era. Dr. Jin received Young Investigator Grant from Southeastern Center for Electrical Engineering Education (SCEEE) in 2015, early CAREER award from Department of Energy (DoE) in 2016, Outstanding New Faculty Award (ONFA) from ACM's Special Interest Group on Design Automation (SIGDA) in 2017, and Young Investigator Award (YIP) from Office of Naval Research (ONR) in 2019. He also received the Best Paper Award of the 52nd Design Automation Conference in 2015, the 21st Asia and South Pacific Design Automation Conference (DAC) in 2016, the 10thIEEE Symposium on Hardware-Oriented Security and Trust (HOST) in 2017, the 2018 ACM Transactions on Design Automation of Electronic Systems (TODAES), the 28thedition of the ACM Great Lakes Symposium on VLSI (GLSVLSI) in 2018, and the Design, Automation and Test in Europe Conference and Exhibition (DATE) in 2019. He is the IEEE Council on Electronic Design Automation (CEDA) Distinguished Lecturer.

10:00 – 11:00
Title: **Low power analog circuits for biomedical applications**
Speaker: **Pieter Harper** - Eindhoven University of Technology (Netherlands)

Chair: **Juan Castellano** (UTFPR, SSCS member)

Abstract:

Electronics play an important role to enable the next generation of medical devices, like wearables, implants, or other invasive devices. These applications usually demand miniaturization and a low power consumption. In this talk, a couple of example applications are described, after which we will focus on various design techniques to develop low-power electronic systems and circuits for biomedical instrumentation and imaging. As will become clear, there are many optimizations at various levels (system, circuit, layout, algorithm, analog, and digital) that can be done to get the best possible results. In the last part of the presentation, a concrete design example of an integrated circuit for very low-power electrocardiography recording is discussed in detail, together with in-vivo measurement results.

Biography

Pieter Harpe received the M.Sc. and Ph.D. degrees from the Eindhoven University of Technology in The Netherlands, in 2004 and 2010, respectively. He worked for several years at Holst Centre / imec, The Netherlands. In April 2011, he joined Eindhoven University of Technology where he is currently an Associate Professor on low-power mixed-signal circuits. Dr. Harpe is co-organizer of the yearly workshop on Advances in Analog Circuit Design (AACD) and analog subcommittee chair for the ESSCIRC conference. He also served as ISSCC ITPC member and IEEE SSCS Distinguished Lecturer and is recipient of the ISSCC 2015 Distinguished Technical Paper Award.

11:15 – 12:15
Title: **Trends on EDA**
Speaker: **Ricardo Reis** – Federal University of Rio Grande do Sul (Brazil)
Chair: **José Azambuja** – Chair of the IEEE CASS Rio Grande do Sul Chapter

Abstract:

The design quality of modern chips depends on the quality of the EDA tools used in the design flow. With the evolution of nanotechnologies new EDA tools are needed. Some trends on EDA to cope with the evolution of manufacturing processes will be presented. An important set of EDA tools nowadays are the ones to reduce power consumption at all levels of design abstraction. Power Optimization is fundamental in the IoT world. At logic and physical level, it is needed to reduce the transistor count to reduce leakage power. Also, the use of estimation tools and visualization tools are more and more important in modern design flows.

Biography

Ricardo Reis received a Bachelor degree in Electrical Engineering from Federal University of Rio Grande do Sul (UFRGS), Porto Alegre, Brazil, in 1978, and a Ph.D. degree in Microelectronics from the National Polytechnic Institute of Grenoble (INPG), France, in 1983. Doctor Honoris Causa by the University of Montpellier in 2016. He is a full professor at the Informatics Institute of Federal University of Rio Grande do Sul. His main research includes physical design automation, design methodologies, fault tolerant systems and microelectronics education. He has more than 700 publications including books, journals and conference proceedings. He was vice-president of IFIP (International Federation for Information Processing) and he was also president of the Brazilian Computer Society (two terms) and vice-president of the Brazilian Microelectronics Society. He is an active member of CASS and he received the 2015 IEEE CASS Meritorious Service Award. He was vice-president of CASS for two terms (2008/2011). He is the founder of the Rio Grande do Sul CAS Chapter, which got the World CASS Chapter of The Year Award 2011, 2012, and 2018, and R9 Chapter of The Year 2013, 2014, 2016, 2017 and 2020. He is a founder of several conferences like SBCCI and LASCAS, the CASS Flagship Conference in Region 9. He was the General or Program Chair of several conferences like IEEE ISVLSI, SBCCI, IFIP VLSI-SoC, ICECS, PATMOS. Ricardo was the Chair of the IFIP/IEEE VLSI-SoC Steering Committee, vice-chair of the IFIP WG10.5 and he is Chair of IFIP TC10. He also

proposed and was the first EIC of the Journal of Integrated Circuits and Systems -JICS. He also started with the EMicro, an annually microelectronics school in South Brazil. In 2002 he received the Researcher of the Year Award in the state of Rio Grande do Sul. He is a founding member of the SBC (Brazilian Computer Society) and also founding member of SBMicro (Brazilian Microelectronics Society). He was member of CASS DLP Program (2014/2015), and he has done more than 70 invited talks in conferences. Member of IEEE CASS BoG and IEEE CEDA BoG.

13:45 – 15:00 (Joint talk with SBMicro Mini-Colloquium)
Title: Quantum Computing in Nanoscale CMOS using Position-Based Charge Qubits
Speakers: **Elena Blokhina and Robert Bogdan Staszewski**

Abstract

Quantum computing is a new paradigm that exploits fundamental principles of quantum mechanics, such as superposition and entanglement, to tackle problems in mathematics, chemistry and material science that are well beyond the reach of supercomputers. Despite the intensive worldwide race to build a useful quantum computer, it is projected to take decades before reaching the state of useful quantum supremacy. The main challenge is that qubits operate at the atomic level, thus are extremely fragile, and difficult to control and read out. The current state-of-art implements a few dozen magnetic-spin based qubits in a highly specialized technology and cools them down to a few tens of millikelvin. The high cost of cryogenic cooling prevents its widespread use. A companion classical electronic controller, needed to control and read out the qubits, is mostly realized with room-temperature laboratory instrumentation. This makes it bulky and nearly impossible to scale up to the thousands or millions of qubits needed for practical quantum algorithms. We propose a new quantum computer paradigm that exploits the wonderful scaling achievements of mainstream integrated circuits (IC) technology which underpins personal computers and mobile phones. Just like with a small IC chip, where a single nanometer-sized CMOS transistor can be reliably replicated millions of times to build a digital processor, we propose a new structure of a qubit realized as a CMOS-compatible charge-based quantum dot that can be reliably replicated thousands of times to construct a quantum processor. Combined with an on-chip CMOS controller, it will realize a useful quantum computer which can operate at a much higher temperature of 4 kelvin.

Biographys

Elena Blokhina received the Habilitation HDR (equiv. D.Sc.) degree in electronic engineering from UPMC Sorbonne Universities, France, in 2017, the Ph.D. degree in physical and mathematical sciences and the M.Sc degree in physics from Saratov State University, Russia, in 2006 and 2002 respectively. Since 2007, she has been with the School of Electrical and Electronic Engineering of University College Dublin, Ireland, and is currently an Associate Professor and the coordinator of the Circuits and Systems Research Group. Prof Blokhina is a Senior member of IEEE and the Chair of the IEEE Technical Committee on Nonlinear Circuits and Systems. She had been elected to serve as a member of the Boards of Governors of the IEEE Circuits and Systems Society for the term 2013-2015 and has been re-elected for the term 2015-2017. In 2016-2017 Prof Blokhina was an Associate Editor for IEEE Transactions on Circuits and Systems I, and since 2018 she is the Deputy Editor in Chief of that Journal. Her research interests include the design, theory and modelling of micro/quantum systems and electronics. She is CTO Equal1 Labs Ireland aiming at building a CMOS quantum computer.

R. Bogdan Staszewski received his PhD from University of Texas at Dallas, USA in 2002. He joined Texas Instruments in Dallas, Texas in 1995. In 1999 he co-started a Digital RF Processor (DRP) group in TI with a mission to invent new digitally intensive approaches to traditional RF functions. Dr. Staszewski served as a CTO of the DRP group between 2007 and 2009. In July 2009 he joined Delft University of Technology in the Netherlands. Since Sept. 2014 he is a Full Professor at University College Dublin (UCD) in Ireland. He has co-authored 130 journal and 200 conference publications, and holds 200 issued US patents. His research interests include nanoscale CMOS architectures and circuits for frequency synthesizers, transmitters and receivers, as well as quantum computers. He is a co-founder of a startup company Equal1 Labs aiming at building the first practical CMOS quantum computer. He is an IEEE Fellow and a recipient of IEEE Circuits and Systems Industrial Pioneer Award.

15:15 – 16:30
Title: **Fully open source manufacturable PDK for a 130nm pro**cess
Speaker: **Tim 'mithro' Ansell** – Google (USA)
Chair: **Omar Parnaiba Vilela Neto** – SBC/CECCI Coordinator

Abstract:

Last year, Google, SkyWater and efabless have partnered to launch a shuttle program based on SkyWater's SKY130 open-source process (130 nm CMOS). This technology is offered to the open community along with a complete design flow to enable designers to implement their ideas. This talk will provide an overview of this program and highlight upcoming opportunities to benefit from it. Finally, it will showcase specific design work delivered by the community members and articulate a call to action for volunteers to design, teach and mentor.

Biography:

Tim 'mithro' Ansell is a software engineer at Google and has been developing open source software for 20+ years. Tim has recently started trying to shake things up in the hardware accelerator development ecosystem by removing roadblocks to having a completely open ecosystem. Recently he worked with SkyWater Foundry to release a fully open source, manufacturable PDK for their 130nm process node and is funding a free shuttle program for open source designs. He has also contributed to projects in the open EDA ecosystem like OpenROAD, OpenRAM, Magic and many others.