

## SBMicro – EDS/IEEE Mini-colloquium

8:45 – 9:45

"Modeling and Simulation of FinFET and Nanosheet Transistors for Advanced Technology Nodes", *Yogesh Chauhan*

### Abstract

### Biography:

Yogesh Singh Chauhan is a professor at Indian Institute of Technology Kanpur, India. He was with Semiconductor Research & Development Center at IBM Bangalore during 2007 – 2010; Tokyo Institute of Technology in 2010; University of California Berkeley during 2010-2012; and ST Microelectronics during 2003-2004. He is the developer of several industry standard models: ASM-GaN-HEMT model, BSIM-BULK (formerly BSIM6), BSIM-CMG, BSIM-IMG, BSIM4 and BSIM-SOI models. His research group is involved in developing compact models for GaN transistors, FinFET, Nanosheet/Gate-All-Around FETs, FDSOI transistors, Negative Capacitance FETs and 2D FETs. His research interests are characterization, modeling, and simulation of semiconductor devices.

He is the Fellow of IEE, Editor of IEEE Transactions on Electron Devices and Distinguished Lecturer of the IEEE Electron Devices Society. He is the member of IEEE-EDS Compact Modeling Committee and fellow of Indian National Young Academy of Science (INYAS). He is the founding chairperson of IEEE Electron Devices Society U.P. chapter and Vice-chairperson of IEEE U.P. section. He has published more than 200 papers in international journals and conferences.

He received Ramanujan fellowship in 2012, IBM faculty award in 2013 and P. K. Kelkar fellowship in 2015, CNR Rao faculty award, Humboldt fellowship and Swarnajayanti fellowship in 2018. He has served in the technical program committees of IEEE International Electron Devices Meeting (IEDM), IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), IEEE European Solid-State Device Research Conference (ESSDERC), IEEE Electron Devices Technology and Manufacturing (EDTM), and IEEE International Conference on VLSI Design and International Conference on Embedded Systems.



**10:00 – 11:00**

**“Hexagonal boron nitride based electronic devices and circuits: status and prospects”, Mario Lanza**

**Abstract:** Memristors have attracted enormous interest due to their excellent capability to store digital information, and they are being considered to be a key element to build future artificial neural networks for bio-inspired neuromorphic computing systems. Recent works have shown that memristors made of layered two-dimensional (2D) materials can exhibit performances that traditional memristors (made of transition metal oxides) do not show, such as excellent transparency and flexibility, high-temperature stability, and unique controllability of the conductance potentiation, depression and relaxation. However, most studies on 2D materials based memristors focused on single devices, and system level performances like yield and device-to-device variability have never been analyzed in depth, despite the great interest that they have raised. In this talk, I will present the first wafer-scale statistical analysis of high-density memristive crossbar arrays made of 2D layered materials, their nanoscale electronic characterization with conductive atomic force microscopy, and their application to neuromorphic computing.

**Biography:** Mario Lanza is an Associate Professor of Materials Science and Engineering at the King Abdullah University of Science and Technology (KAUST), in Saudi Arabia since October 2020. Dr. Lanza got his PhD in Electronic Engineering with honors in 2010 at Universitat Autònoma de Barcelona. During the PhD he was a visiting scholar at The University of Manchester (UK) and Infineon Technologies (Germany). In 2010-2011 he was NSFC postdoc at Peking University, and in 2012-2013 he was Marie Curie postdoc at Stanford University. On October 2013 he joined Soochow University as Associate Professor, and in March 2017 he was promoted to Full Professor. Prof. Lanza has published over 120 research papers, including Science, Nature Electronics, Nature Chemistry, and IEDM, edited a book for Wiley-VCH, and registered four patents (one of them granted with 5.6 Million CNY). Prof. Lanza has received the 2017 Young Investigator Award from Microelectronic Engineering (Elsevier), and the 2015 Young 1000 Talent award (among others), and in 2019 he was appointed as Distinguished Lecturer of the Electron Devices Society (IEEE-EDS). Prof. Lanza is Associate Editor of Scientific Reports (Nature) and Microelectronic Engineering (Elsevier), and serves in the board of many others, like Advanced Electronic Materials (Wiley-VCH), Nanotechnology and Nano Futures (IOP). He is also an active member of the technical committee of several world-class international conferences, including IEEE-IEDM, IEEE-IRPS, IEEE-IPFA and APS. Prof. Lanza leads a research group formed by 10-15 PhD students and postdocs, and they investigate how to improve electronic devices using 2D materials, with special emphasis on two-dimensional (layered) dielectrics and memristors for non-volatile digital information storage and artificial intelligence computing systems.



**11:15 – 12:15**

**From CMOS to neuromorphic Computing, with a peek into the future”, Merlyne De Souza**

**Abstract**

At the heart of the electronics revolution lies a three-terminal transistor: the humble Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). Scaling of this transistor according to Moore’s law has had a transformative effect on society, giving us products from computers, laptops to smart phones, that have made life virtually unrecognisable from 50 years ago. This talk will focus on the physics of operation of the MOSFET leading towards present day challenges of sub-threshold operation such as negative capacitance FETs. Combining memory with CMOS presents one possible pathway for massively parallel and highly energy efficient neuromorphic computing systems of the future.

**Biography**

Maria Merlyne De Souza received her PhD from the University of Cambridge. She became Professor of Electronics and Materials at the Emerging Technologies Research Centre, De Montfort University in 2003 and Professor of Microelectronics at the University of Sheffield in 2007. She has been a technical and executive committee member of IEEE- International Electron Devices Meeting between 2012-2017 and a technical committee member of the IEEE-International Reliability Physics Symposium 2003-2013. She is currently technical committee member of the European Microwave Conference, ESREF, ISPS etc. She has published over 100 journal papers and 150 conferences.



**13:45 – 15:00 (Joint talk with SBCCI Mini-Colloquium)**

**Title: Quantum Computing in Nanoscale CMOS using Position-Based Charge Qubits**

**Speakers: Elena Blokhina and Robert Bogdan Staszewski**

### **Abstract**

Quantum computing is a new paradigm that exploits fundamental principles of quantum mechanics, such as superposition and entanglement, to tackle problems in mathematics, chemistry and material science that are well beyond the reach of supercomputers. Despite the intensive worldwide race to build a useful quantum computer, it is projected to take decades before reaching the state of useful quantum supremacy. The main challenge is that qubits operate at the atomic level, thus are extremely fragile, and difficult to control and read out. The current state-of-art implements a few dozen magnetic-spin based qubits in a highly specialized technology and cools them down to a few tens of millikelvin. The high cost of cryogenic cooling prevents its widespread use. A companion classical electronic controller, needed to control and read out the qubits, is mostly realized with room-temperature laboratory instrumentation. This makes it bulky and nearly impossible to scale up to the thousands or millions of qubits needed for practical quantum algorithms. We propose a new quantum computer paradigm that exploits the wonderful scaling achievements of mainstream integrated circuits (IC) technology which underpins personal computers and mobile phones. Just like with a small IC chip, where a single nanometer-sized CMOS transistor can be reliably replicated millions of times to build a digital processor, we propose a new structure of a qubit realized as a CMOS-compatible charge-based quantum dot that can be reliably replicated thousands of times to construct a quantum processor. Combined with an on-chip CMOS controller, it will realize a useful quantum computer which can operate at a much higher temperature of 4 kelvin.

### **Biographys**

Elena Blokhina received the Habilitation HDR (equiv. D.Sc.) degree in electronic engineering from UPMC Sorbonne Universities, France, in 2017, the Ph.D. degree in physical and mathematical sciences and the M.Sc degree in physics from Saratov State University, Russia, in 2006 and 2002 respectively. Since 2007, she has been with the School of Electrical and Electronic Engineering of University College Dublin, Ireland, and is currently an Associate Professor and the coordinator of the Circuits and Systems Research Group. Prof Blokhina is a Senior member of IEEE and the Chair of the IEEE Technical Committee on Nonlinear Circuits and Systems. She had been elected to serve as a member of the Boards of Governors of the IEEE Circuits and Systems Society for the term 2013-2015 and has been re-elected for the term 2015-2017. In 2016-2017 Prof Blokhina was an Associate Editor for IEEE Transactions on Circuits and Systems I, and since 2018 she is the Deputy Editor in Chief of that Journal. Her research interests include the design, theory and modelling of micro/quantum systems and electronics. She is CTO Equal1 Labs Ireland aiming at building a CMOS quantum computer.



R. Bogdan Staszewski received his PhD from University of Texas at Dallas, USA in 2002. He joined Texas Instruments in Dallas, Texas in 1995. In 1999 he co-started a Digital RF Processor (DRP) group in TI with a mission to invent new digitally intensive approaches to traditional RF functions. Dr. Staszewski served as a CTO of the DRP group between 2007 and 2009. In July 2009 he joined Delft University of Technology in the Netherlands. Since Sept. 2014 he is a Full Professor at University College Dublin (UCD) in Ireland. He has co-authored 130 journal and 200 conference publications, and holds 200 issued US patents. His research interests include nanoscale CMOS architectures and circuits for frequency synthesizers, transmitters and receivers, as well as quantum computers. He is a co-founder of a startup company Equal1 Labs aiming at building the first practical CMOS quantum computer. He is an IEEE Fellow and a recipient of IEEE Circuits and Systems Industrial Pioneer Award.



**15:15 – 16:30**

**Heterogeneous Integration for AI Architectures, *Mukta Farooq***

**Abstract**

While silicon scaling has reached astonishing levels over the last half century, there has not been a corresponding level of scaling in electronic packaging technology. However, Artificial Intelligence (AI) architectures are now changing the landscape, increasingly moving us towards advanced packaging technology, especially Heterogeneous Integration (HI). What are these unique requirements of AI which are driving the need for HI? What are some of the unique challenges in semiconductor and packaging technologies that must be overcome to make this successful?

This seminar will discuss these questions, and discuss various heterogeneous integration methods and their characteristics, including interposers, fan out wafer level processing, silicon bridges, and 3D integration. We will look at their attributes as well as their challenges, to determine how they can be leveraged to achieve AI architectures.

**Biography:**

Dr. Mukta Farooq is a Distinguished Research Staff Member at IBM Research. She is an IEEE Fellow, an IEEE EDS Distinguished Lecturer, and a Distinguished Alumna of IIT-Bombay (India). Mukta is a materials scientist with expertise in Heterogeneous and 3D Integration, CMOS BEOL, and Chip Package Interaction. Mukta received the IBM Outstanding Technical Achievement Award for the semiconductor industry's first high volume 3D logic wafer. Mukta has 222 granted US patents and numerous publications. She is an IBM Lifetime Master Inventor and an IBM Academy of Technology member. Mukta received her BS from IIT-Bombay, MS from Northwestern University, and PhD from Rensselaer Polytechnic Institute.

